1. FEATURES

• **CPU**

8 Bit CISC Core(8051 Compatible)

• **ROM capacity**

9K Bytes, Flash with self read/write capability
On chip debug and In-system programming (ISP)
Endurance: 10,000 times (Sector 0 to 279)
100,000 times (Sector 280 to 287)

• **SRAM capacity**

256 Bytes (IRAM)
(Including LCD display RAM, 34 Bytes)

• **General Purpose I/O (GPIO)**

Normal I/O : 13 I/O
LCD shared I/O : 36 I/O

• **Basic Interval Timer (BIT)**

8Bit × 1ch

• **Watch Dog Timer (WDT)**

8Bit × 1ch
5KHz internal RC oscillator

• **Timer/ Counters**

8Bit × 4ch (T0/T1/T2/T3) or 16Bit x 2ch (T0/T2)
16Bit x 1ch (T4)

• **Programmable Pulse Generation**

Carrier generation (by T1), T2 Clock source
Pulse generation (by T4)

• **Watch Timer (WT)**

3.91mS/0.25S/0.5S/1S interval at 32.768KHz

• **Buzzer**

8Bit x 1ch

• **SIO**

8Bit x 1ch

• **UART**

8Bit x 1ch

• **10 Bit A/D Converter**

8 Input channels
20uS conversion time

• **LCD Driver**

28 Segments and 8 Common terminals
30kΩ , 60kΩ and 120kΩ internal dividing resistor selectable
1/2, 1/3, 1/4, 1/5, 1/6 and 1/8 duty selectable
1/2, 1/3, and 1/4 bias selectable

• **Power On Reset**

Reset release level (1.4V)

• **Low Voltage Reset**

14 level detect (1.60V, 2.0V,,,,,, 4.4V)

• **Low Voltage Indicator**

13 level detect (2.0V,,,,,, 4.4V)

• **Interrupt Source**

External Interrupts (EINT10, EINT12, EINT14),
Key Interrupts (8 inputs)
T0,,,,4, WDT, WT, BIT, UART, SIO, ADC

• **Internal RC Oscillator**

Frequency: 16MHz ± 1.5% (@0℃ ~ 50℃)

• **Power Down Mode**

Stop and Idle mode

• **Operating Voltage & Frequency**

1.8V to 5.5V @ 32 to 38KHz with X-tal
1.8V to 5.5V @ 0.4 to 4.2MHz with Ceramic
2.0V to 5.5V @ 0.4 to 4.2MHz with X-tal
2.7V to 5.5V @ 0.4 to 12.0MHz with X-tal
2.0V to 5.5V @ 0.5 to 16MHz with IRC and PLL

• **Minimum Instruction Execution Time**

125nS at 16MHz CPU clock

• **Operating Temperature**

–40 to +85℃

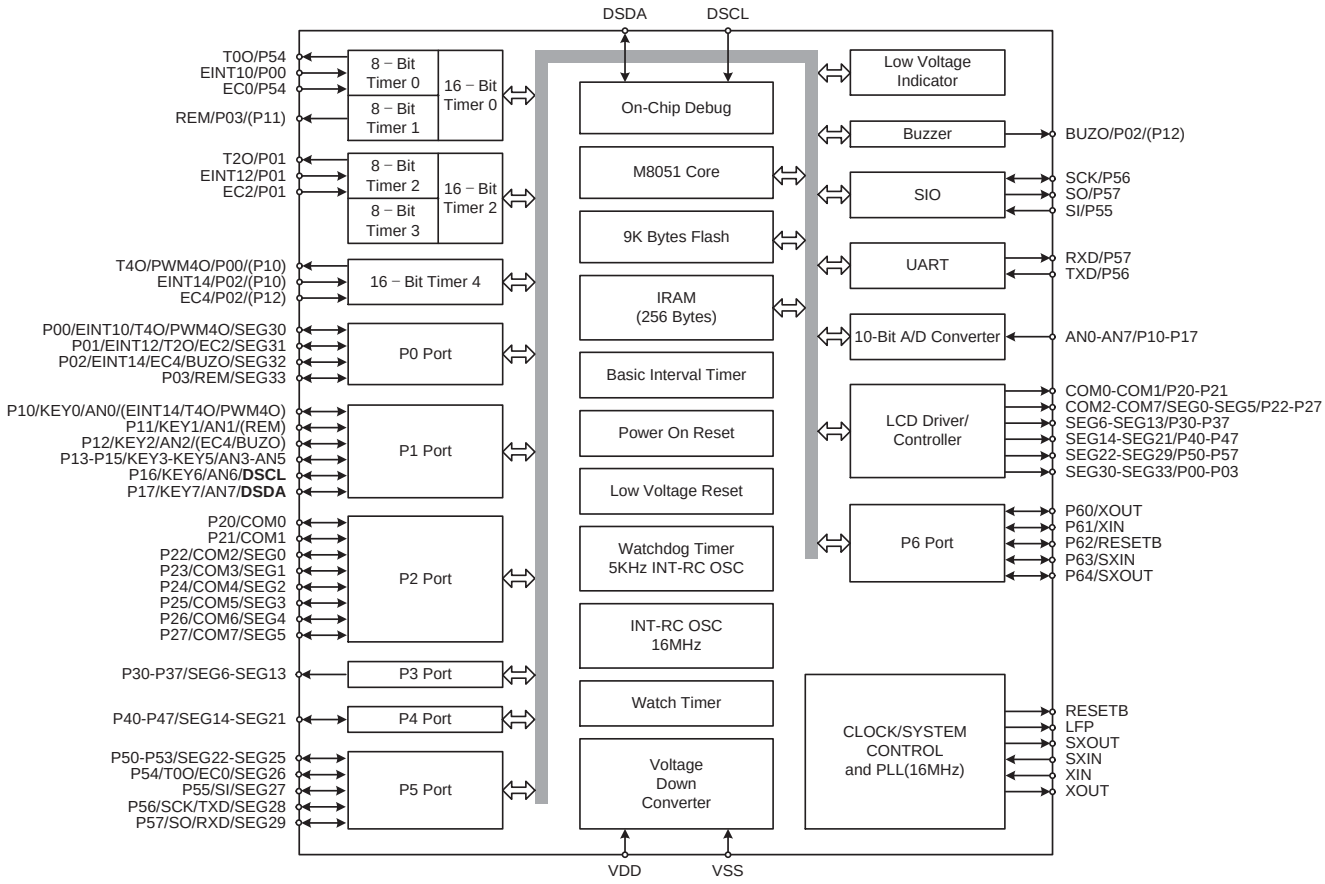
• **Oscillator Type**

0.4-12MHz crystal or ceramic for main clock
32.768Hz crystal for sub clock
Phase locked loop (Max. 16MHz with sub clock)

• **Package**

52-Pin Pellet, 48-Pin LQFP, Pb-free package

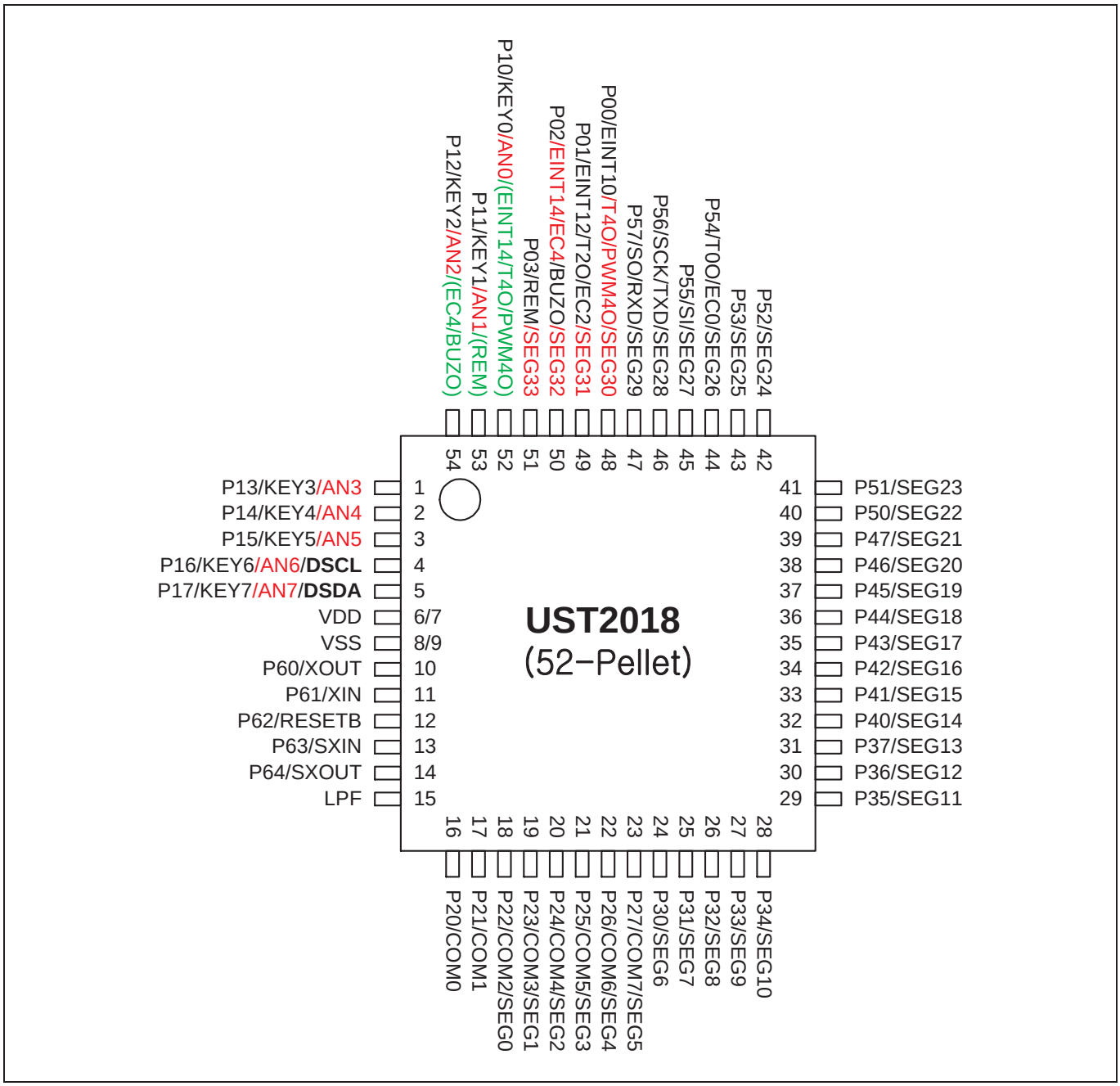
2. BLOCK DIAGRAM



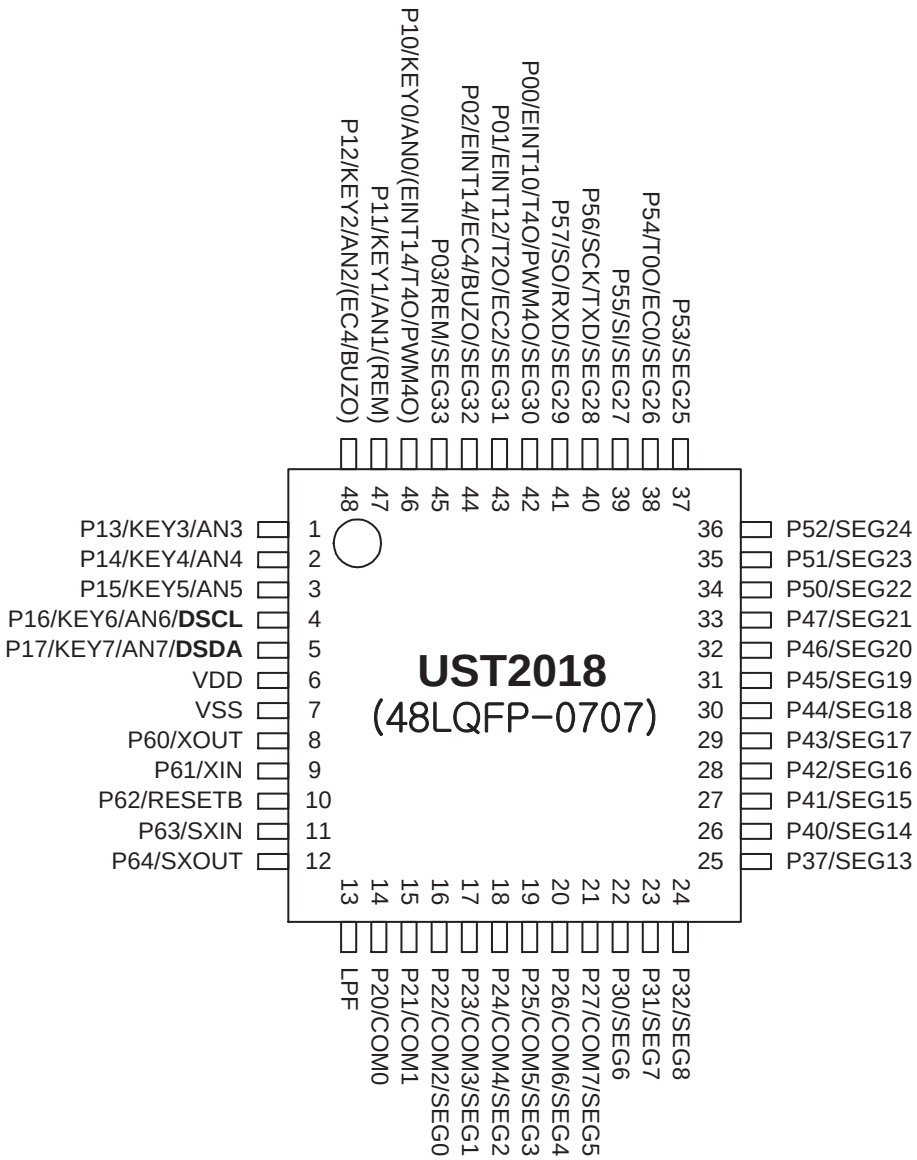
Note: The P33-P36 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 48-pin package is used.

3. PIN ASSIGNMENTS

3.1 52 PIN-PELLET



3.2 48 PIN-LQFP



Note: The P33-P36 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 48-pin package is used.

4. PIN DESCRIPTIONS

Pin Names	I/O	Pin Description	After RESET	Alternative Functions
P00	I/O	Port 0 except P03 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	EINT10/T4O/ PWM4O/SEG30
P01				EINT12/T2O/ EC2/SEG31
P02				EINT14/EC4/ BUZO/SEG32
P03	I/O	The P03 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	REM/SEG33
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	KEY0/AN0/(EINT14/T4O/ PWM4O)
P11				KEY1/AN1/(REM)
P12				KEY2/AN2/(EC4/BUZO)
P13–P15				KEY3–KEY5/AN3–AN5
P16				KEY6/AN6/DSCL
P17				KEY7/AN7/DSDA
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	COM0
P21				COM1
P22–P27				COM2–COM7/ SEG0–SEG5
P30–P37	I/O	Port 3 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P33-P36 are not in the 48-Pin package.	Input	SEG6–SEG13
P40–P47	I/O	Port 4 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SEG14–SEG21
P50–P53	I/O	Port 5 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SEG22–SEG25
P54				T0O/EC0/SEG26
P55				SI/SEG27
P56				SCK/TXD/SEG28
P57				SO/RXD/SEG29
P60	I/O	Port 6 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	XOUT
P61				XIN
P62				RESETB
P63				SXIN
P64				SXOUT

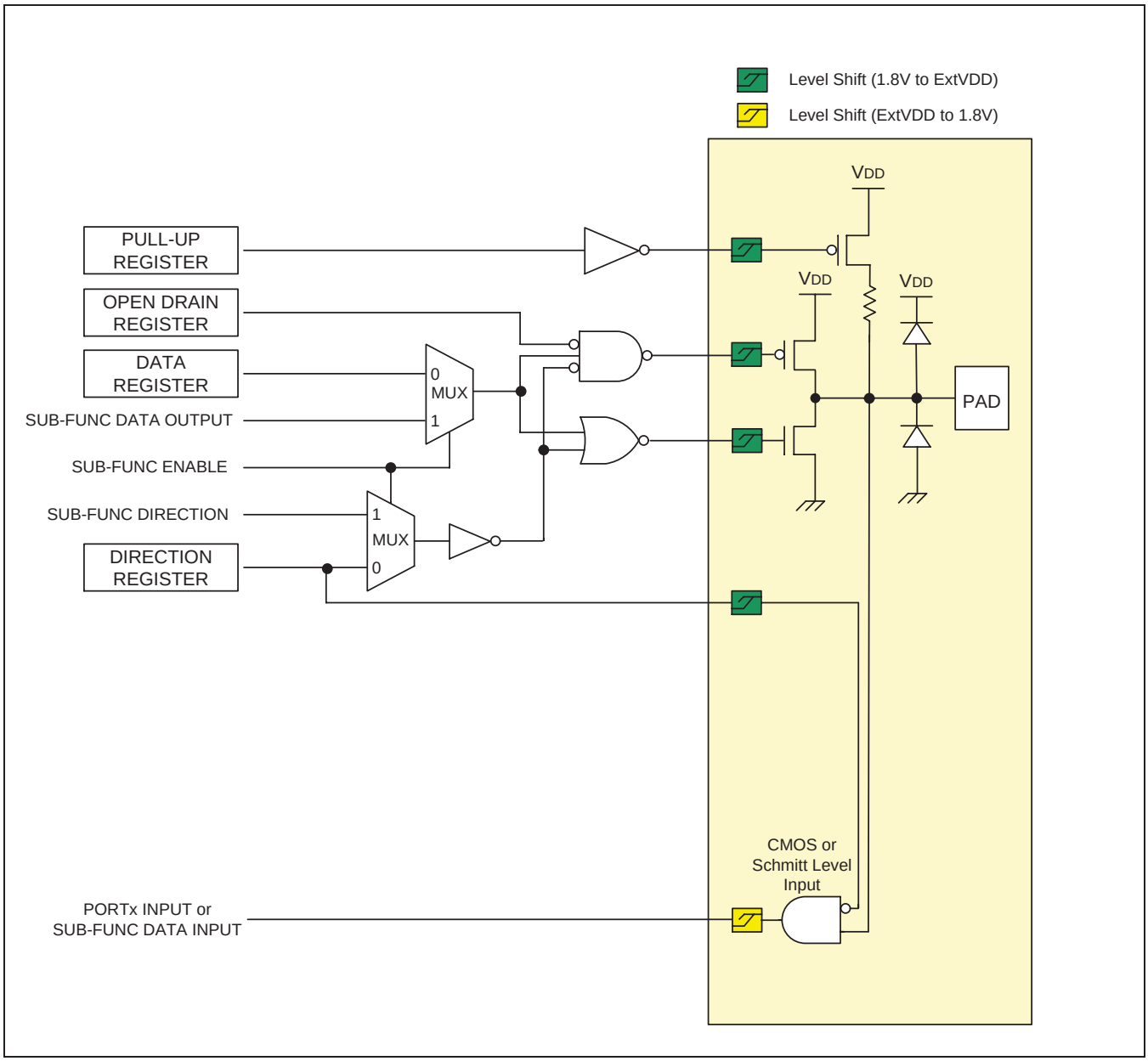
Pin Names	I/O	Pin Description	After RESET	Alternative Functions
EINT10	I/O	External interrupt input and Timer 0 capture input	Input	P00/T4O/ PWM4O/SEG30
EINT12	I/O	External interrupt input and Timer 2 capture input	Input	P01/T2O/EC2 /SEG31
EINT14	I/O	External interrupt input and Timer 4 capture input	Input	P02/EC4/ BUZO/SEG32
KEY0	I/O	External Key interrupt input	Input	P10/AN0/(EINT14/ T4O/PWM4O)
KEY1				P11/AN1/(REM)
KEY2				P12/AN2/ (EC4/BUZO)
KEY3				P13/AN3
KEY4				P14/AN4
KEY5				P15/AN5
KEY6				P16/AN6/DSCL
KEY7				P17/AN7/DSDA
T0O	I/O	Timer 0 interval output	Input	P54/EC0/SEG26
T2O	I/O	Timer 2 interval output	Input	P01/EINT12/EC2/SE31
T4O	I/O	Timer 4 interval output	Input	P00/EINT10/PWM4O/ SEG30/(P10)
EC0	I/O	Timer 0 event count input	Input	P54/T0O/SEG26
EC2	I/O	Timer 2 event count input	Input	P01/EINT12/T2O/SEG31
EC4	I/O	Timer 4 event count input	Input	P02/EINT14/BUZO/ SEG32/(P12)
REM	I/O	Carrier generation output	Input	P03/SEG33/(P11)
BUZO	I/O	Buzzer signal output	Input	P02/EINT14/EC4/ SEG32/(P12)
SCK	I/O	Serial clock input/output	Input	P56/TXD/SEG28
SI	I/O	Serial data input	Input	P55/SEG27
SO	I/O	Serial data output	Input	P57/RXD/SEG29
TXD	I/O	UART data output	Input	P56/SCK/SEG28
RXD	I/O	UART data input	Input	P57/SO/SEG29
AN0	I/O	A/D converter analog input channels	Input	P10/KEY0/ (EINT14/T4O/PWM4O)
AN1				P11/KEY1/(REM)
AN2				P12/KEY2/ (EC4/BUZO)
AN3–AN5				P13–P15/KEY3–KEY5
AN6				P16/KEY6/DSCL
AN7				P17/KEY7/DSDA

Pin Names	I/O	Pin Description	After RESET	Alternative Functions
COM0–COM1	I/O	LCD common signal output	Input	P20–P21
COM2–COM7				P22–P27/ SEG0–SEG5
SEG0–SEG5	I/O	LCD Segment signal output	Input	P22–P27/ COM2–COM7
SEG6–SEG21				P30–P47
SEG22–SEG25				P50–P53
SEG26				P54/T0O/EC0
SEG27				P55/SI
SEG28				P56/SCK/TXD
SEG29				P57/SO/RXD
SEG30				P00/EINT10/ T4O/PWM4O
SEG31				P01/EINT12/ T2O/EC2
SEG32				P02/EINT14/ EC4/BUZO
SEG33				P03/REM
DSDA	I/O	On chip debugger data input/output (Note 4)	Input	P17/KEY7
DSCL	I/O	On chip debugger clock input (Note 4)	Input	P16/KEY6
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION	Input	P62
XIN	I/O	Main oscillator pins	Input	P61
XOUT				P60
SXIN	I/O	Sub oscillator pins.	Input	P63
SXOUT				P64
LPF	–	Loop filter pump output for PLL	–	–
VDD, VSS	–	Power input pins	–	–

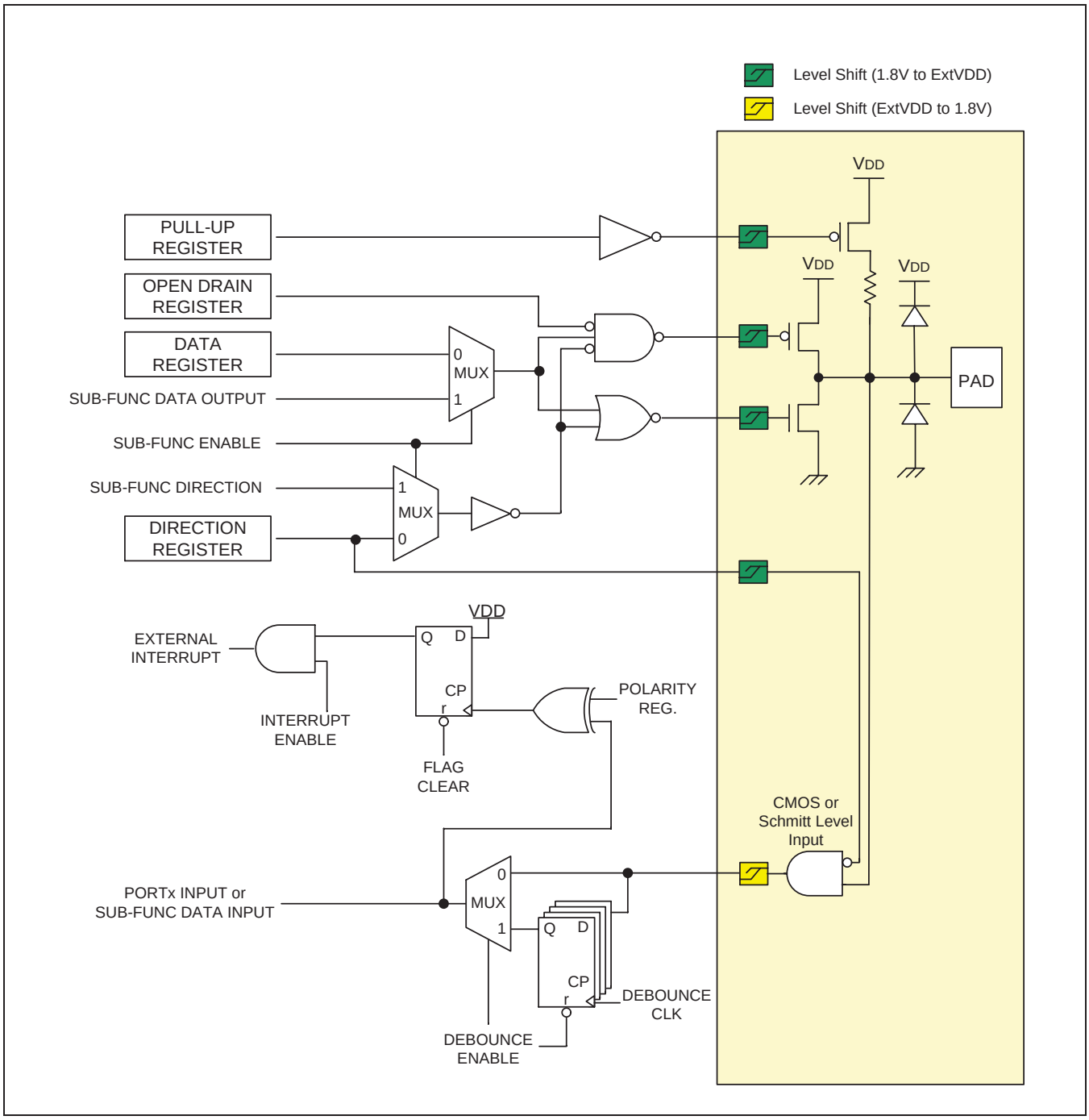
Notes: 1. The P33-P36 are not in the 48-Pin package.
2. The P62/RESETB pin is configured as one of the P62 and the RESETB pin by the "CONFIGURE OPTION".
3. If the P16/DSCL and P17/DSDA pins are connected to an emulator during power-on reset, the pins are automatically configured as the debugger pins.
4. The P16/DSCL and P17/DSDA pins are configured as inputs with internal pull-up resistors during the reset or power-on reset.
5. The P60/XOUT, P61/XIN, P63/SXIN, and P64/SXOUT pins are configured as a function pin by software control.

5. PORT STRUCTURES

5.1 GENERAL PURPOSE I/O PORT



5.2 EXTERNAL INTERRUPT I/O PORT



6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit	Note
Supply Voltage	VDD	-0.3 – +6.5	V	–
Normal Pin	V_I	-0.3 – V_{DD}+0.3	V	Voltage on any pin with respect to Vss
	V_O	-0.3 – V_{DD}+0.3	V	
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	Σ I_{OH}	-80	mA	Maximum current (Σ I_{OH})
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	Σ I_{OL}	120	mA	Maximum current (Σ I_{OL})
Total Power Dissipation	T_P	600	mW	–
Storage Temperature	T_{STG}	-65 – +150	°C	–

6.2 RECOMMENDED OPERATING CONDITIONS

(T_A = - 40 °C to + 85°C)

Parameter	Symbol	Conditions		Min	Max	Units
Operating Voltage	V_{DD}	fx = 32 – 38KHz	SX-tal	1.8	5.5	V
		fx = 0.4 – 4.2MHz	Ceramic	1.8	5.5	
		fx = 0.4 – 4.2MHz	X-tal	2.0	5.5	
		fx = 0.4 – 12MHz		2.7	5.5	
		fx = 0.5 – 8MHz	Internal RC	1.8	5.5	
		fx = 0.5 – 16MHz		2.0	5.5	
		fx = 0.5 – 16MHz	PLL	2.0	5.5	
Operating Temperature	T_{OPR}	V_{DD} = 1.8 – 5.5V		-40	85	°C

6.3 POWER-ON RESET CHARACTERISTICS

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 – 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset Release Level	V_{POR}	–	–	1.4	–	V
V_{DD} Voltage Rising Time	t_R	–	0.05	–	30.0	V/mS
POR Current	I_{POR}	–	–	0.2	–	uA

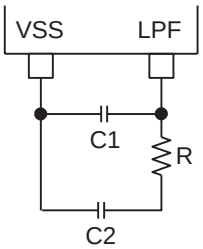
6.4 LOW VOLTAGE RESET AND LOW VOLTAGE INDICATOR CHARACTERISTICS

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 – 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.60V.		–	1.60	1.79	V
				1.85	2.00	2.15	
				1.95	2.10	2.25	
				2.05	2.20	2.35	
				2.17	2.32	2.47	
				2.29	2.44	2.59	
				2.39	2.59	2.79	
				2.55	2.75	2.95	
				2.73	2.93	3.13	
				2.94	3.14	3.34	
				3.18	3.38	3.58	
				3.37	3.67	3.97	
				3.70	4.00	4.30	
				4.10	4.40	4.70	
Hysteresis	△V	–		–	50	150	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	uS
LVR and LVI Current	I_{BL}	Enable (Both)	V_{DD}=3V, Run mode	–	14.0	24.0	uA
		Enable (One of two)		–	10.0	18.0	
		Disable (Both)	V_{DD}=3V	–	–	0.1	

6.5 PHASE LOCKED-LOOP CHARACTERISTICS

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 – 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Frequency Range	–		–	32.768	–	kHz
Output Frequency Range	f_{VCO}		0.5	–	16	MHz
Clock Duty Ratio	T_{OD}		45	50	55	%
Tolerance	–		–	–	±4.0	%
Settling Time	t_D		–	10	100	mS
PLL Current	I_{PLL}	Enable, f_{VCO}=16MHz	–	0.5	1.0	mA
		Disable	–	–	0.1	uA

Note: Where R= 6.8kΩ, C1=820pF, and C2= 10nF.

6.6 A/D CONVERTER CHARACTERISTICS

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 – 5.5V, V_{SS}=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Resolution	–	–		–	10	–	bit
Integral Linear Error	ILE	VDD=2.7V – 5.5V, fx=8MHz		–	–	±5	LSB
Differential Linearity Error	DLE			–	–	±1	
Zero Offset Error	ZOE			–	–	±5	
Full Scale Error	FSE			–	–	±5	
Conversion Time	tCON	10bit resolution, fx=8MHz		20	–	–	uS
Analog Input Voltage	VAN	–		VSS	–	VDD	V
A/DC Input Leakage Current	IAN	VDD=5.12V		–	–	2	uA
A/DC Current	IADC	Enable	VDD=5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

Notes: 1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS);
2. Full scale error is the difference between 111111111111 and the converted output for full-scale input voltage (VDD).
3. When VDD is lower than 2.7V, the ADC resolution is worse.

6.7 INTERNAL RC OSCILLATOR CHARACTERISTICS

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 – 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Frequency	fIRC	VDD = 2.0V to 5.5V		–	16	–	MHz
Tolerance	–	T_A = 0 °C to + 50 °C	With 0.1uF Bypass capacitor	–	–	±1.5	%
		T_A = – 20 °C to + 85 °C		–	–	±2.5	
		T_A = – 40 °C to + 85 °C		–	–	±3.5	
Clock Duty Ratio	TOD	–		40	50	60	%
Stabilization Time	tFS	–		–	–	100	uS
IRC Current	IIRC	Enable		–	0.2	–	mA
		Disable		–	–	0.1	uA

Note: A 0.1uF bypass capacitor should be connected to VDD and VSS. Refer to the “Recommended Circuit and Layout".

6.8 INTERNAL WATCH-DOG TIMER RC OSCILLATOR CHARACTERISTICS

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 – 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	fWDTRC	–	2	5	10	kHz
Stabilization Time	tWDTS	–	–	–	1	mS
WDTRC Current	IWDTRC	Enable	–	1	–	uA
		Disable	–	–	0.1	

6.9 LCD VOLTAGE CHARACTERISTICS

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 – 5.5V, Vss=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
LCD Voltage	VLC0	LCD contrast disabled, 1/4 bias		Typx0.95	VDD	Typx1.05	V
		LCD contrast enabled, 1/4 bias, RLCD1, No panel load, VDD = 2.7V to 5.5V	LCDCCR=00H	Typx0.9	VDDx16/31	Typx1.1	V
			LCDCCR=01H		VDDx16/30		
			LCDCCR=02H		VDDx16/29		
			LCDCCR=03H		VDDx16/28		
			LCDCCR=04H		VDDx16/27		
			LCDCCR=05H		VDDx16/26		
			LCDCCR=06H		VDDx16/25		
			LCDCCR=07H		VDDx16/24		
			LCDCCR=08H		VDDx16/23		
			LCDCCR=09H		VDDx16/22		
			LCDCCR=0AH		VDDx16/21		
			LCDCCR=0BH		VDDx16/20		
			LCDCCR=0CH		VDDx16/19		
			LCDCCR=0DH		VDDx16/18		
			LCDCCR=0EH		VDDx16/17		
			LCDCCR=0FH		VDDx16/16		
LCD Mid Bias Voltage(note)	VLC1	VDD = 2.7V to 5.5V, LCD clock = 0Hz, 1/4 bias, No panel load		Typ-0.2	3/4xVLC0	Typ+0.2	V
	VLC2			Typ-0.2	2/4xVLC0	Typ+0.2	
	VLC3			Typ-0.2	1/4xVLC0	Typ+0.2	
LCD Driver Output Impedance	RLO	VLCD=3V, ILOAD=±10uA		–	5	10	kΩ
LCD Bias Dividing Resistor	RLCD1	T_A = 25°C		20	30	40	
	RLCD2			40	60	80	
	RLCD3			80	120	160	

Note: It is middle output voltage when the VDD and the VLC0 node are connected.

6.10 DC ELECTRICAL CHARACTERISTICS

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 – 5.5V, Vss=0V, f_{XIN}=12MHz)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input High Voltage	VIH1	P00 – P03, P1, P6, RESETB		0.8VDD	–	VDD	V
	VIH2	All input pins except VIH1		0.7VDD	–	VDD	
Input Low Voltage	VIL1	P00 – P03, P1, P6, RESETB		–	–	0.2VDD	V
	VIL2	All input pins except VIL1		–	–	0.3VDD	
Output High Voltage	VOH	VDD=4.5V, IOH = – 2mA; All output ports		VDD-1.0	–	–	V
Output Low Voltage	VOL	VDD=4.5V, IOL = 15mA; All output ports		–	–	1.0	V
Input high leakage current	IIH	All Input ports		–	–	1.0	uA
Input low leakage current	IIL	All Input ports		– 1.0	–	–	uA
Pull-up resistor	R_{PU1}	VI=0V, TA=25°C, All Input ports	VDD=5V	25	50	100	kΩ
			VDD=3V	50	100	200	
	R_{PU2}	VI=0V, TA=25°C, RESETB	VDD=5V	150	250	400	kΩ
			VDD=3V	300	500	700	
OSC feedback resistor	RX1	XIN=VDD, XOUT=VSS, TA=25°C, VDD=5V		600	1200	2000	kΩ
	RX2	SXIN=VDD, SXOUT=VSS, TA=25°C, VDD=5V		2500	5000	10000	
Supply current	IDD1 (RUN)	f_{XIN} =12MHz	VDD=5V±10%	–	3.0	6.0	mA
		f_{XIN} =10MHz	VDD=3V±10%	–	2.2	4.4	
		f_{IRC}=16MHz	VDD=5V±10%	–	3.0	6.0	
	IDD2 (IDLE)	fxin=12MHz	VDD=5V±10%	–	1.3	2.6	mA
		fxin=10MHz	VDD=3V±10%	–	0.7	1.4	
		f_{IRC}=16MHz	VDD=5V±10%	–	0.8	1.6	
	IDD3	f_{SUB}=32.768KHz, VDD=3V±10%, TA=25°C	Sub Run	–	60.0	90.0	uA
	IDD4		Sub Idle	–	8.0	16.0	uA
	IDD5	Stop, VDD=5V±10%, TA=25°C		–	0.5	3.0	uA

Notes: 1. Where the f_{XIN} is an external main oscillator, the f_{SUB} is an external sub oscillator, the f_{IRC} is an internal RC oscillator, and the fx is the selected system clock.
2. All supply current items don't include the current of an internal watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

6.11 AC CHARACTERISTICS

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESETB input low width	t_{RST}	V_{DD} = 5 V	10	–	–	uS
Interrupt Input High, Low width	t_{IWH}, t_{IWL}	All interrupts, V_{DD} = 5 V	200	–	–	nS
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	ECn, V_{DD} = 5 V (n=0, 2, and 4)	200	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	ECn, V_{DD} = 5 V (n=0, 2, and 4)	20	–	–	
REM port High, Low width	t_{REMWH}, t_{REMWL}	REM, V_{DD} = 5 V	5	–	–	uS

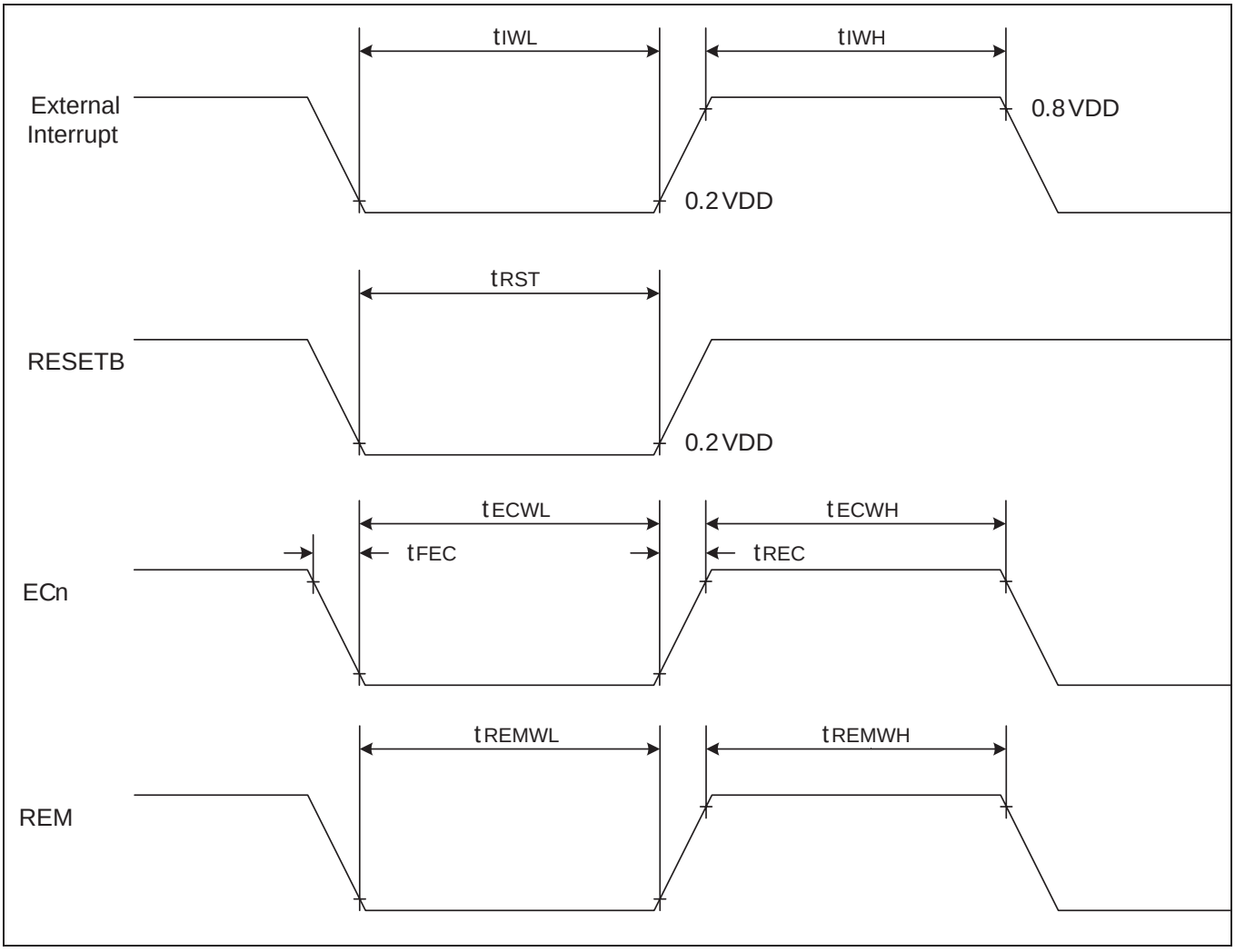


Figure 6–1. AC Timing

6.12 SERIAL I/O CHARACTERISTICS

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SCK cycle time	t_{KCY}	External SCK source	1,000	–	–	nS
		Internal SCK source	1,000			
SCK high, low width	t_{KH}, t_{KL}	External SCK source	500			nS
		Internal SCK source	t_{KCY}/2–50			
SI setup time to SCK high	t_{SIK}	External SCK source	250			nS
		Internal SCK source	250			
SI hold time to SCK high	t_{KSI}	External SCK source	400			nS
		Internal SCK source	400			
Output delay for SCK to SO	t_{KSO}	External SCK source	–	–	300	nS
		Internal SCK source			250	

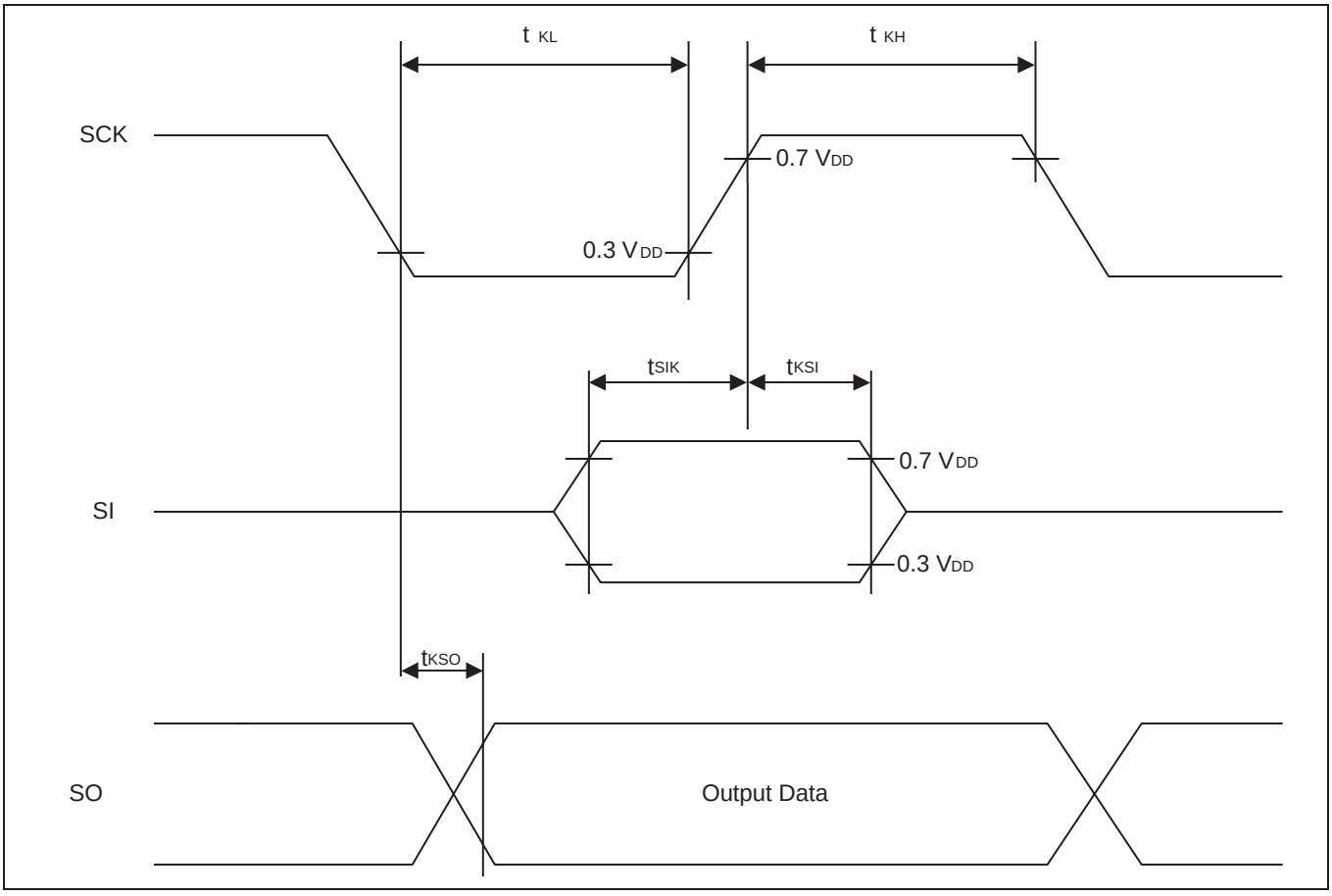


Figure 6–2. Serial Interface Data Transfer Timing

6.13 UART TIMING CHARACTERISTICS

(T_A = - 40°C to +85°C, V_{DD} = 1.8 V to 5.5 V, f_{XIN}=11.1MHz)

Parameter	Symbol	Min	Typ	Max	Units
Serial port clock cycle time	t_{SCK}	1250	$t_{CPU} \times 16$	1650	nS
Output data setup to clock rising edge	t_{S1}	590	$t_{CPU} \times 13$	–	
Clock rising edge to input data valid	t_{S2}	–	–	590	
Output data hold after clock rising edge	t_{H1}	$t_{CPU} - 50$	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	$t_{CPU} \times 8$	970	

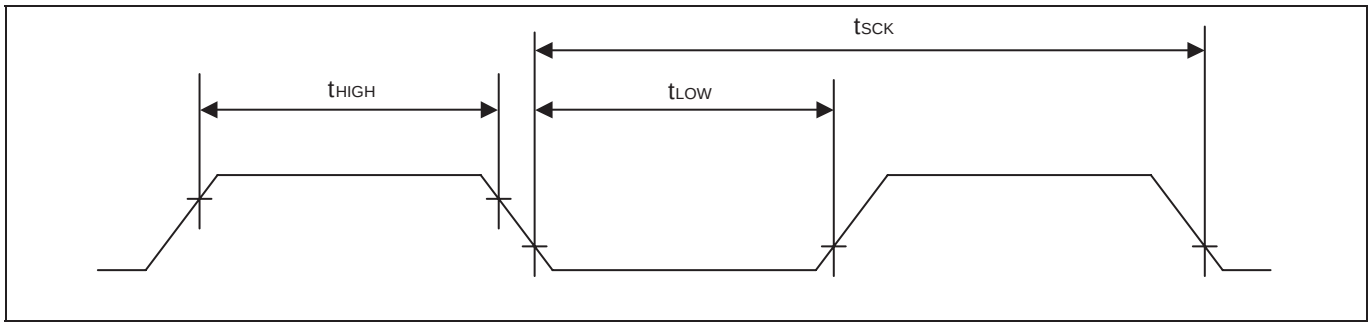


Figure 6–3. Waveform for UART Timing Characteristics

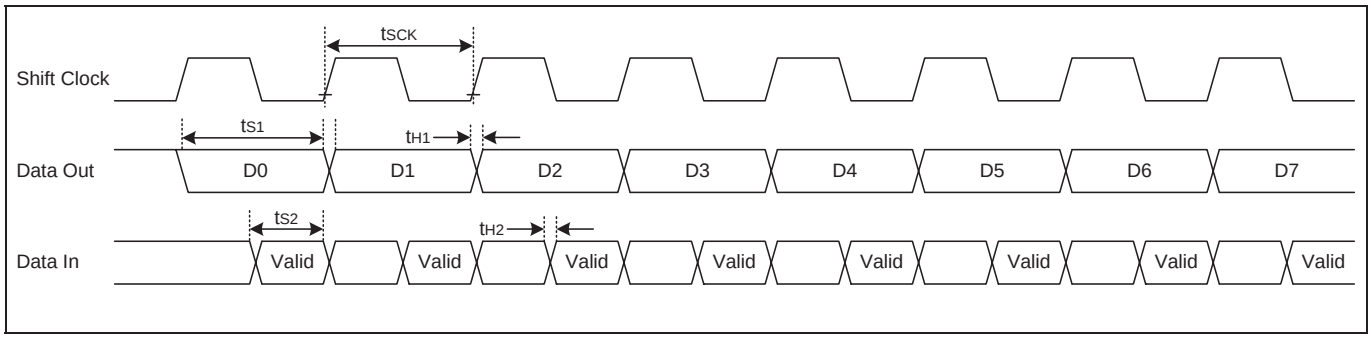
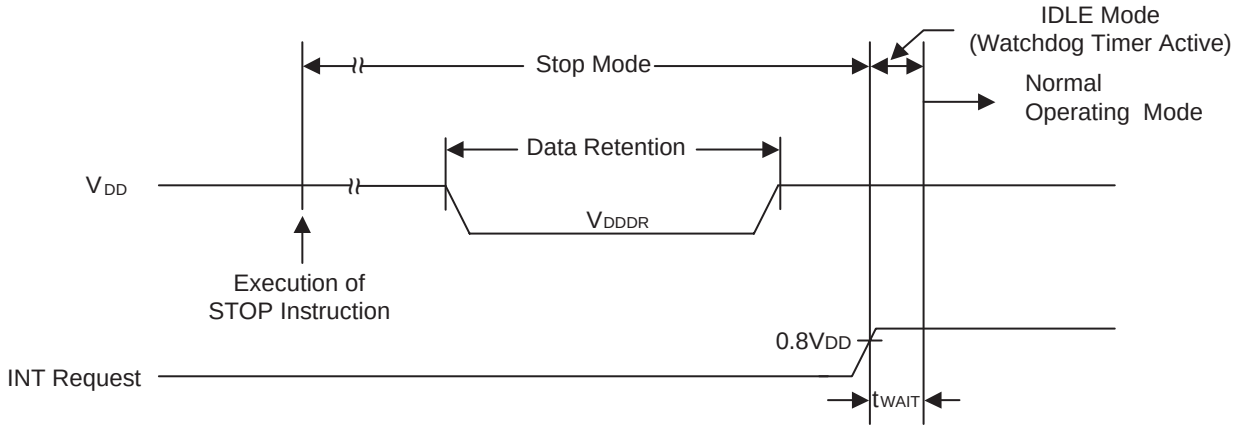


Figure 6–4. Timing Waveform for UART Module

6.14 DATA RETENTION VOLTAGE IN STOP MODE

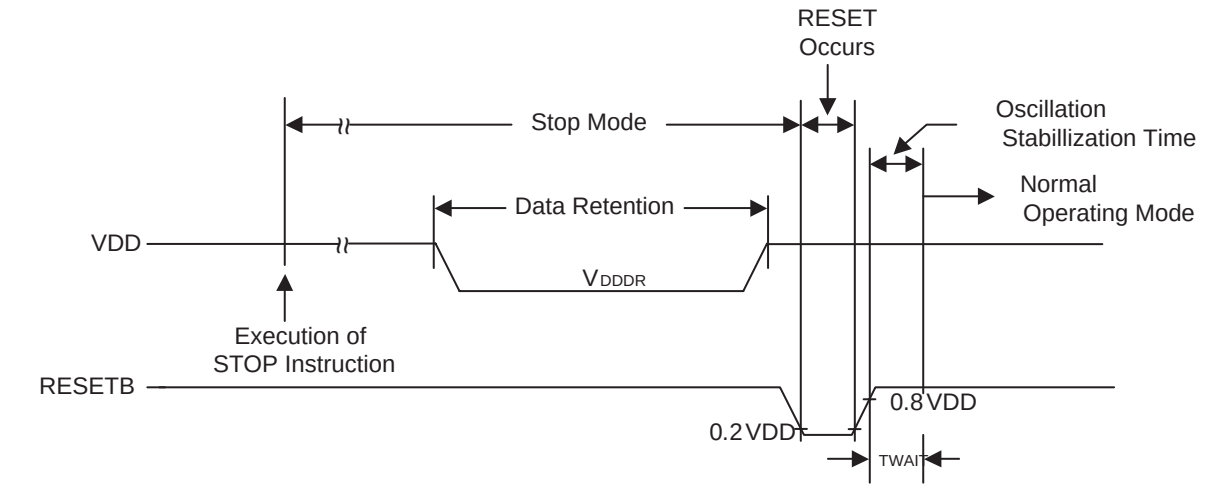
(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8V (T_A = 25 °C), Stop mode	–	–	1	uA



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 6–5. Stop Mode Release Timing When Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 16/f_{IRC}) = (16.4 mS at fx=1MHz).

Figure 6–6. Stop Mode Release Timing When Initiated by RESETB

6.15 INTERNAL FLASH ROM CHARACTERISTICS

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 – 5.5V, Vss=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Sector Write Time	TFSW	–	–	2.5	2.7	mS
Sector Erase Time	TFSE	–	–	2.5	2.7	
Hard-Lock Time	TFHL	–	–	2.5	2.7	
Page Buffer Reset Time	TFBR	–	–	–	5	uS
Flash Programming Frequency	fPGM	–	0.4	–	–	MHz
Endurance of Write/Erase	NFWE	Sector 0 to 279	–	–	10,000	Times
		Sector 280 to 287	–	–	100,000	Times

6.16 INPUT/OUTPUT CAPACITANCE

(T_A = - 40 °C to + 85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Capacitance	CIN	f=1MHz Unmeasured pins are connected to Vss	–	–	10	pF
Output Capacitance	COUT					
I/O Capacitance	CIO					

6.17 MAIN CLOCK OSCILLATOR CHARACTERISTICS

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Crystal	Main oscillation frequency	2.0 V – 5.5 V	0.4	–	4.2	MHz
		2.7 V – 5.5 V	0.4	–	12.0	
Ceramic Oscillator	Main oscillation frequency	1.8 V – 5.5 V	0.4	–	4.2	MHz
		2.7 V – 5.5 V	0.4	–	12.0	
External Clock	X_{IN} input frequency	1.8 V – 5.5 V	0.4	–	4.2	MHz
		2.7 V – 5.5 V	0.4	–	12.0	

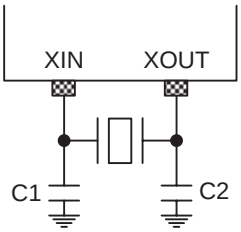


Figure 6–7. Crystal/Ceramic Oscillator

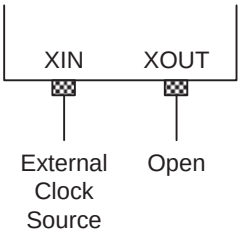


Figure 6–8. External Clock

6.18 SUB CLOCK OSCILLATOR CHARACTERISTICS

((T$_A$ = - 40 ˚C to + 85˚C, V$_{DD}$ = 1.8 V to 5.5 V)

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Crystal	Sub oscillation frequency	1.8 V – 5.5 V	32	32.768	38	kHz
External Clock	SX$_{IN}$ input frequency		32	–	100	kHz

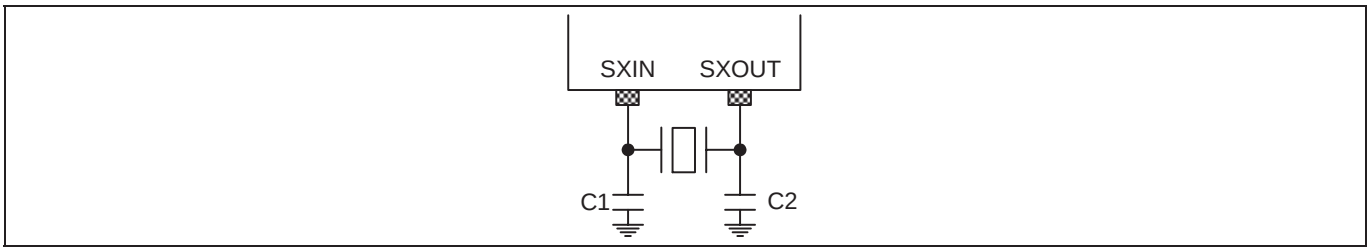


Figure 6–9. Crystal Oscillator

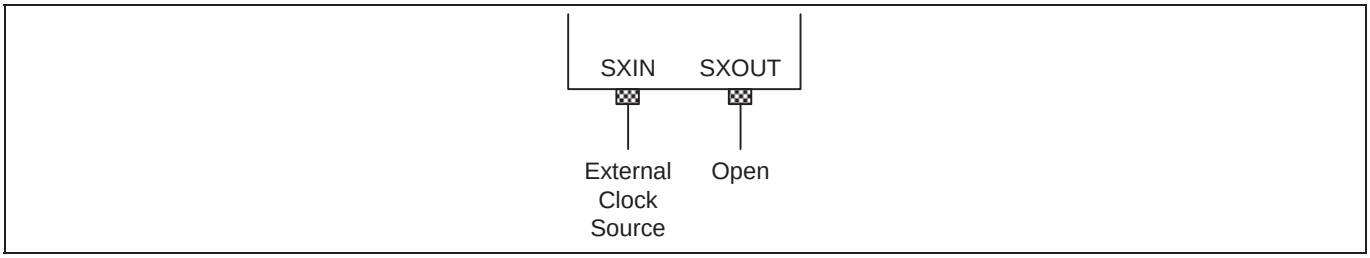


Figure 6–10. External Clock

6.19 MAIN OSCILLATION STABILIZATION TIME

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	f_{XIN} ≥ 1 MHz	–	–	60	mS
Ceramic	Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	10	
External Clock	f_{XIN} = 0.4 to 12 MHz XIN input high and low width (t_{XL}, t_{XH})	42	–	1250	nS

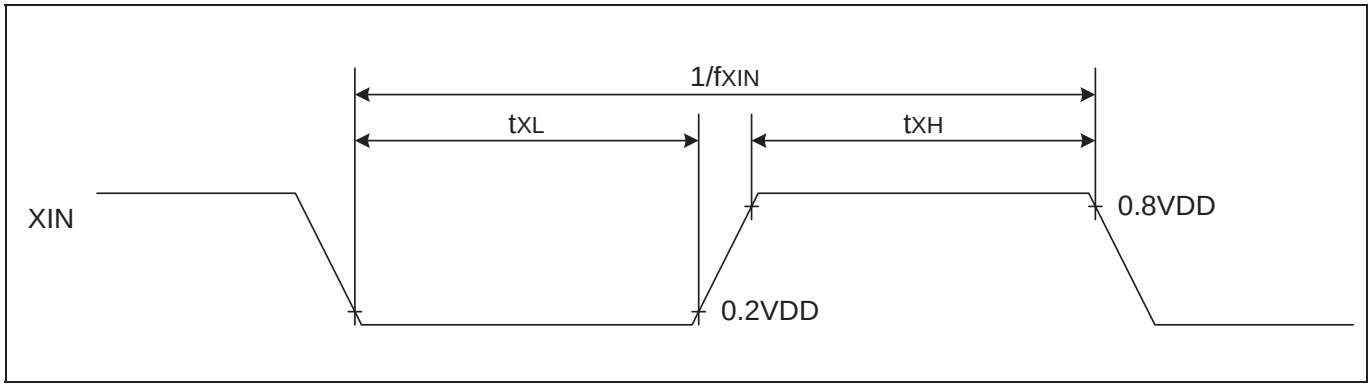


Figure 6–11. Clock Timing Measurement at XIN

6.20 SUB OSCILLATION STABILIZATION TIME

(T_A = - 40 °C to + 85°C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	–	–	–	10	S
External Clock	SXIN input high and low width (t_{XL}, t_{XH})	5	–	15	uS

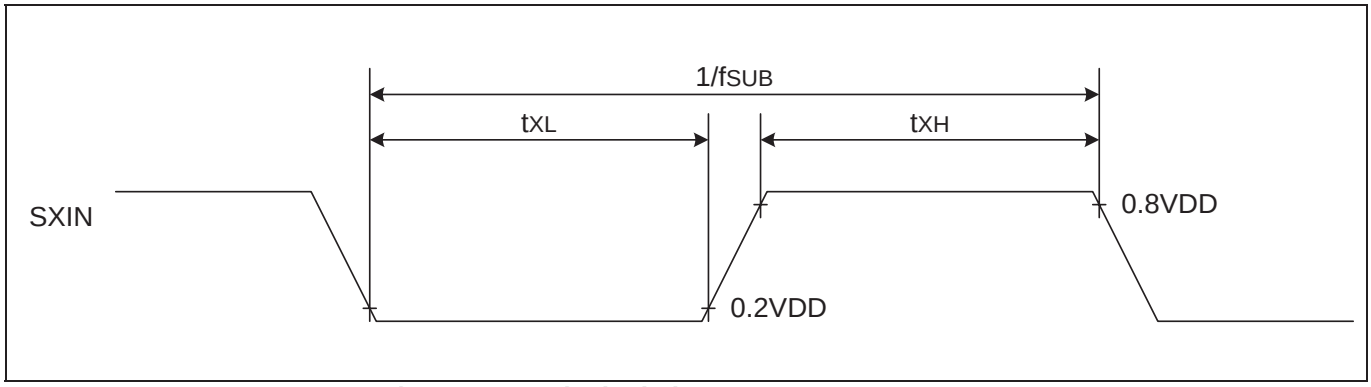


Figure 6–12. Clock Timing Measurement at SXIN

6.21 OPERATING VOLTAGE RANGE

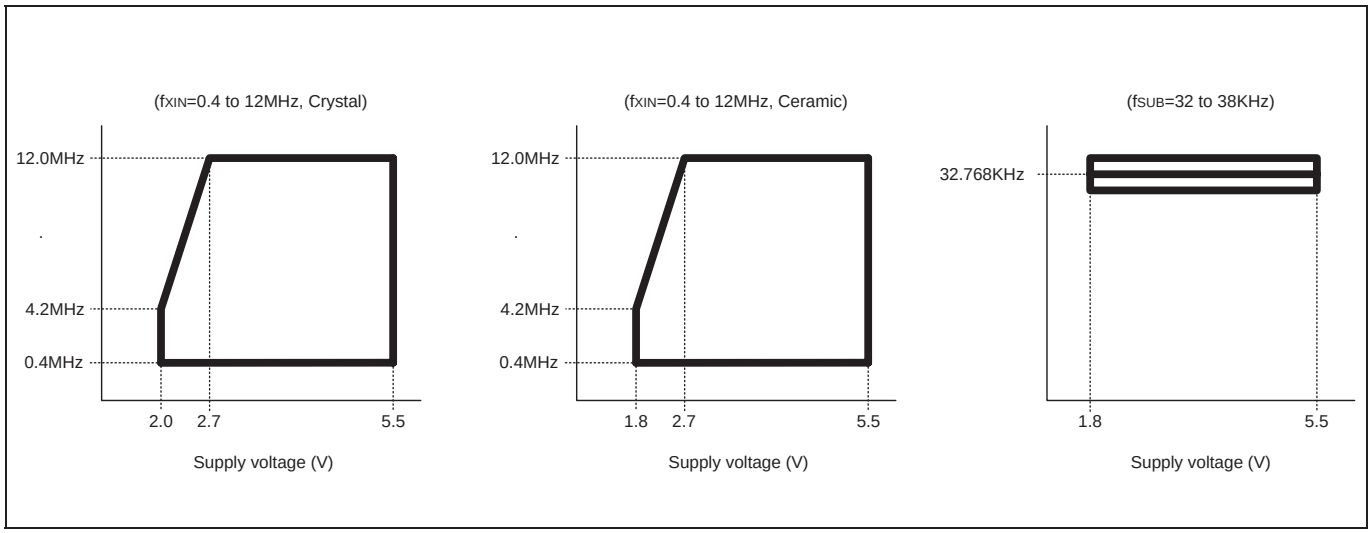


Figure 6–13. Operating Voltage Range

6.22 RECOMMENDED CIRCUIT AND LAYOUT

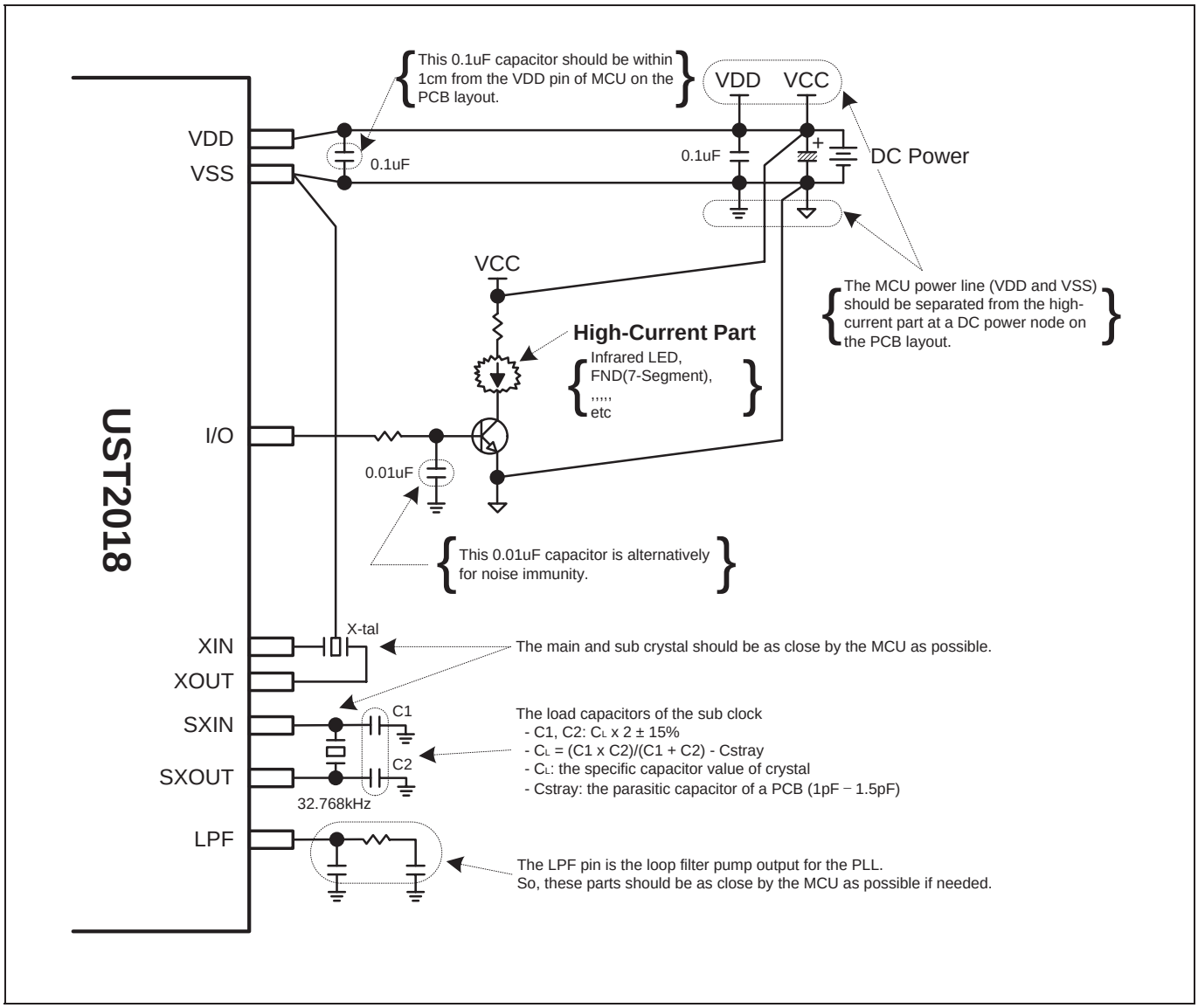
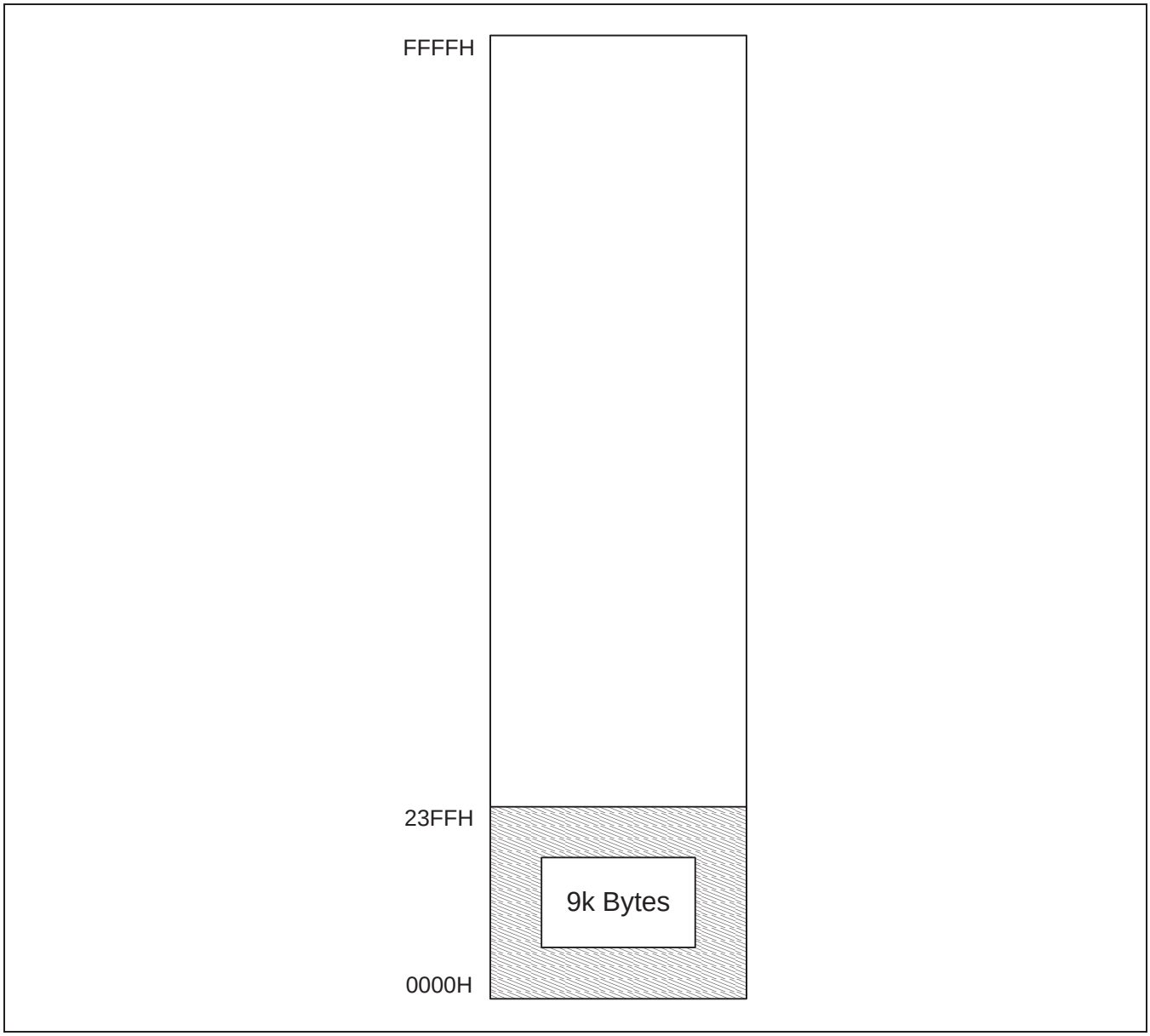


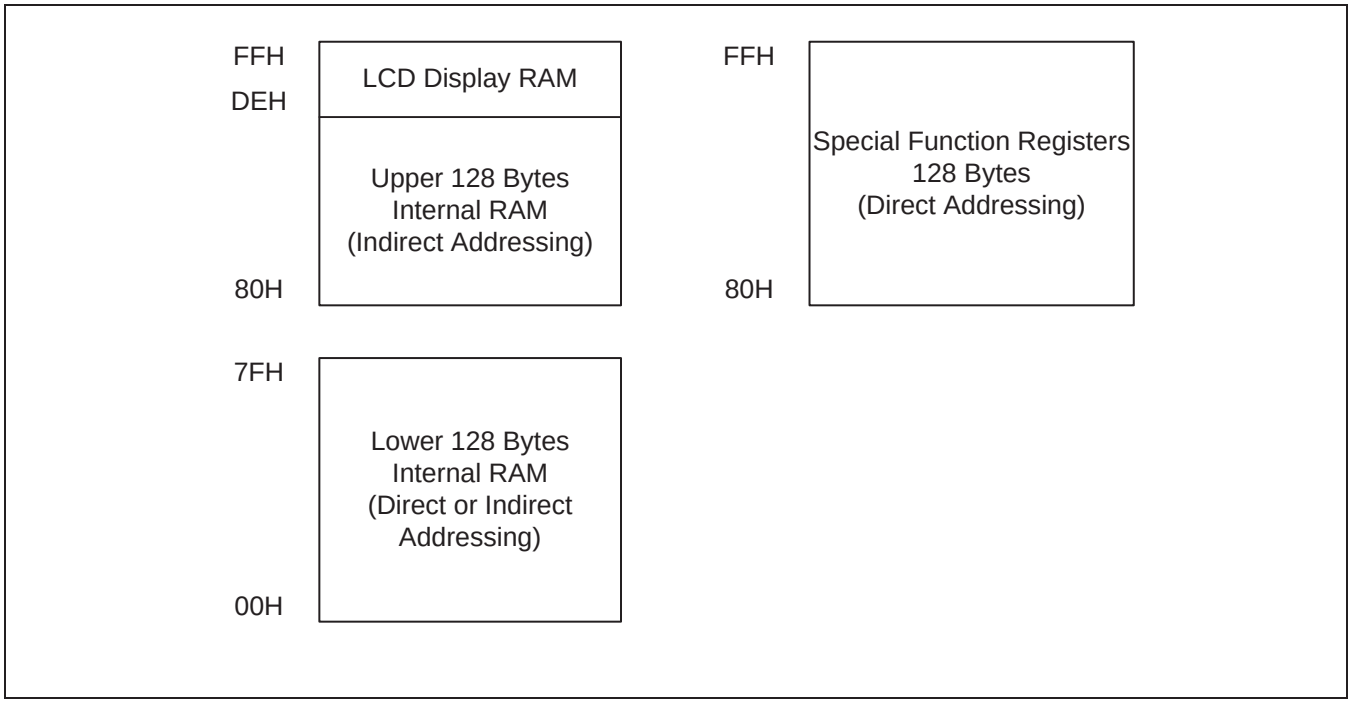
Figure 6–14. Recommended Circuit and Layout

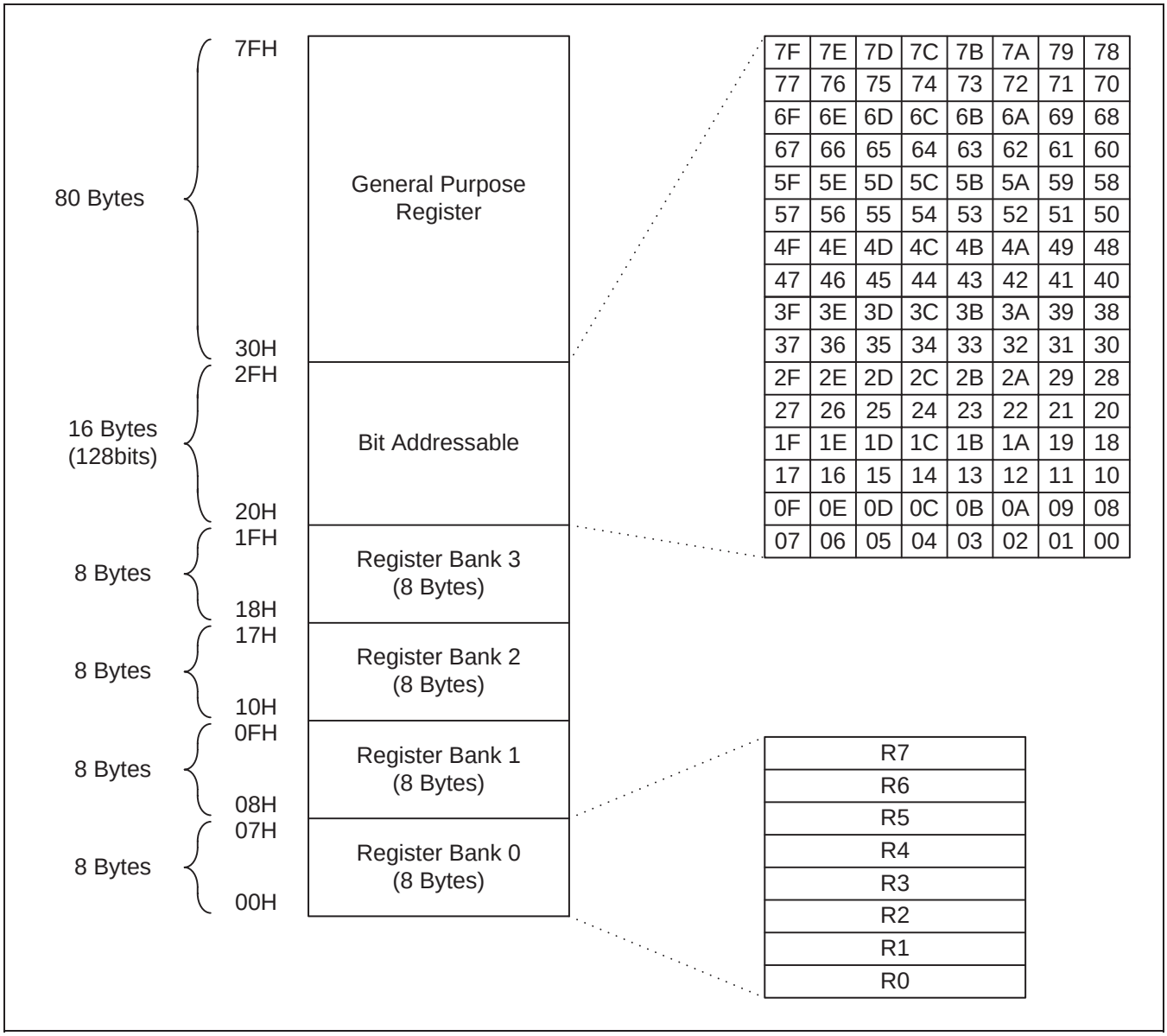
7. MEMORY

7.1 PROGRAM MEMORY



7.2 DATA MEMORY





Lower 128 bytes RAM

7.3 SFR MAP

7.3.1 SFR MAP SUMMARY

- Reserved

M8051 Compatible

	00H/8H(1)	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	**IP1**		FSADRH	FSADRM	FSADRL	FIDR	FMCR	PLLCR
0F0H	**B**	P4FSR	P5FSRL	P5FSRH	P6FSR	LCDCCR	P1FSRL	P1FSRH
0E8H	KFLAG	P0DB	P1DB	LCDCRL	LCDCRH	P0FSR	P2FSR	P3FSR
0E0H	**ACC**	LVICR	UARTCR1	UARTCR2	UARTCR3	UARTST	UARTBD	UARTDR
0D8H	LVRCR	OSCCR	P4PU	P5PU	P6PU		T4BDRL	T4BDRH
0D0H	**PSW**		T4ADRL	T4ADRH	P0PU	P1PU	P2PU	P3PU
0C8H	T4CRL	T4CRH	T1CR	T1CNT	T1DRL	T1DRH/ T1CDR	CARCR	
0C0H	P6	P6IO	T3CR	TIFR	T3CNT		T3DR/ T3CDR	
0B8H	**IP**	P5IO	T2CR		T2CNT		T2DR/ T2CDR	
0B0H	P5	P4IO	T0CR	T0CNT	T0DR/ T0CDR	SIOCR	SIODR	SIOPS
0A8H	**IE**	IE1	IE2	IE3			KPOL0	KPOL1
0A0H	P4	P3IO	**EO**		EIFLAG	EIPOL	ADCDRL	ADCDRH
98H	P3	P2IO	P5OD	P6OD	ADCCRL	ADCCRH	WTCR	WTDR/ WTCNT
90H	P2	P1IO	P0OD	P1OD	P2OD	P3OD	P4OD	BUZCR
88H	P1	P0IO	SCCR	BITCR	BITCNT	WDTCR	WDTDR/ WDTCNT	BUZDR
80H	P0	**SP**	**DPL**	**DPH**	**DPL1**	**DPH1**	RSTFR	**PCON**

Note: (1) These registers are bit-addressable

7.3.2 SFR MAP

Register Name	Mnemonic	Address Hex	R/W	@ RESET							
P0 Data Register	P0	80H	R/W	–	–	–	–	0	0	0	0
Stack Pointer	SP	81H	R/W	0	0	0	0	0	1	1	1
Data Pointer Register Low	DPL	82H	R/W	0	0	0	0	0	0	0	0
Data Pointer Register High	DPH	83H	R/W	0	0	0	0	0	0	0	0
Data Pointer Register Low 1	DPL1	84H	R/W	0	0	0	0	0	0	0	0
Data Pointer Register High 1	DPH1	85H	R/W	0	0	0	0	0	0	0	0
Reset Flag Register	RSTFR	86H	R/W	1	X	0	0	X	–	–	–
Power Control Register	PCON	87H	R/W	0	–	–	–	0	0	0	0
P1 Data Register	P1	88H	R/W	0	0	0	0	0	0	0	0
P0 Direction Register	P0IO	89H	R/W	–	–	–	–	0	0	0	0
System and Clock Control Register	SCCR	8AH	R/W	–	–	–	–	–	–	0	0
Basic Interval Timer Control Register	BITCR	8BH	R/W	0	–	–	–	0	0	0	1
Basic Interval Timer Counter Register	BITCNT	8CH	R	0	0	0	0	0	0	0	0
Watch Dog Timer Control Register	WDTCR	8DH	R/W	0	0	0	–	–	–	0	0
Watch Dog Timer Data Register	WDTDR	8EH	W	1	1	1	1	1	1	1	1
Watch Dog Timer Counter Register	WDTCNT	8EH	R	0	0	0	0	0	0	0	0
BUZZER Data Register	BUZDR	8FH	R/W	1	1	1	1	1	1	1	1
P2 Data Register	P2	90H	R/W	0	0	0	0	0	0	0	0
P1 Direction Register	P1IO	91H	R/W	0	0	0	0	0	0	0	0
P0 Open-drain Selection Register	P0OD	92H	R/W	–	–	–	–	0	0	0	0
P1 Open-drain Selection Register	P1OD	93H	R/W	0	0	0	0	0	0	0	0
P2 Open-drain Selection Register	P2OD	94H	R/W	0	0	0	0	0	0	0	0
P3 Open-drain Selection Register	P3OD	95H	R/W	0	0	0	0	0	0	0	0
P4 Open-drain Selection Register	P4OD	96H	R/W	0	0	0	0	0	0	0	0
BUZZER Control Register	BUZCR	97H	R/W	–	–	–	–	–	0	0	0
P3 Data Register	P3	98H	R/W	0	0	0	0	0	0	0	0
P2 Direction Register	P2IO	99H	R/W	0	0	0	0	0	0	0	0
P5 Open-drain Selection Register	P5OD	9AH	R/W	0	0	0	0	0	0	0	0
P6 Open-drain Selection Register	P6OD	9BH	R/W	–	–	–	0	0	0	0	0
A/D Converter Control Low Register	ADCCRL	9CH	R/W	0	0	–	0	0	–	0	0
A/D Converter Control High Register	ADCCRH	9DH	R/W	0	–	–	–	–	0	0	0
Watch Timer Control Register	WTCR	9EH	R/W	0	–	–	0	0	0	0	0
Watch Timer Data Register	WTDR	9FH	W	0	1	1	1	1	1	1	1
Watch Timer Counter Register	WTCNT	9FH	R	–	0	0	0	0	0	0	0

7.3.3 SFR MAP (CONTINUED)

Register Name	Mnemonic	Address Hex	R/W	@ RESET							
P4 Data Register	P4	A0H	R/W	0	0	0	0	0	0	0	0
P3 Direction Register	P3IO	A1H	R/W	0	0	0	0	0	0	0	0
Extended Operation Register	EO	A2H	R/W	–	–	–	0	–	0	0	0
Reserved		A3H	–								
External Interrupt Flag Register	EIFLAG	A4H	R/W	–	–	–	–	–	0	0	0
External Interrupt Polarity Register	EIPOL	A5H	R/W	–	–	0	0	0	0	0	0
A/D Converter Data Low Register	ADCDRL	A6H	R	x	x	x	x	x	x	x	x
A/D Converter Data High Register	ADCDRH	A7H	R	x	x	x	x	x	x	x	x
Interrupt Enable Register	IE	A8H	R/W	0	–	0	–	0	0	0	–
Interrupt Enable Register 1	IE1	A9H	R/W	–	–	0	0	0	–	–	–
Interrupt Enable Register 2	IE2	AAH	R/W	–	–	0	0	0	0	0	–
Interrupt Enable Register 3	IE3	ABH	R/W	–	–	–	0	0	0	–	0
Reserved		ACH	–								
Reserved		ADH	–								
Key Interrupt Polarity 0 Register	KPOL0	AEH	R/W	0	0	0	0	0	0	0	0
Key Interrupt Polarity 1 Register	KPOL1	AFH	R/W	0	0	0	0	0	0	0	0
P5 Data Register	P5	B0H	R/W	0	0	0	0	0	0	0	0
P4 Direction Register	P4IO	B1H	R/W	0	0	0	0	0	0	0	0
Timer 0 Control Register	T0CR	B2H	R/W	0	0	0	0	0	0	0	0
Timer 0 Counter Register	T0CNT	B3H	R	0	0	0	0	0	0	0	0
Timer 0 Data Register	T0DR	B4H	R/W	1	1	1	1	1	1	1	1
Timer 0 Capture Data Register	T0CDR	B4H	R	0	0	0	0	0	0	0	0
SIO Control Register	SIOCR	B5H	R/W	0	0	0	0	0	0	0	0
SIO Data Register	SIODR	B6H	R/W	0	0	0	0	0	0	0	0
SIO Pre-scaler Register	SIOPS	B7H	R/W	0	0	0	0	0	0	0	0
Interrupt Priority Register	IP	B8H	R/W	–	–	0	0	0	0	0	0
P5 Direction Register	P5IO	B9H	R/W	0	0	0	0	0	0	0	0
Timer 2 Control Register	T2CR	BAH	R/W	0	–	0	0	0	0	0	0
Reserved		BBH	–								
Timer 2 Counter Register	T2CNT	BCH	R	0	0	0	0	0	0	0	0
Reserved		BDH	–								
Timer 2 Data Register	T2DR	BEH	R/W	1	1	1	1	1	1	1	1
Timer 2 Capture Data Register	T2CDR	BEH	R	0	0	0	0	0	0	0	0
Reserved		BFH	–								

7.3.3 SFR MAP (CONTINUED)

Register Name	Mnemonic	Address Hex	R/W	@ RESET							
P6 Data Register	P6	C0H	R/W	–	–	–	0	0	0	0	0
P6 Direction Register	P6IO	C1H	R/W	–	–	–	0	0	0	0	0
Timer 3 Control Register	T3CR	C2H	R/W	0	0	–	0	0	0	0	0
Timer Interrupt Flag Register	TIFR	C3H	R/W	0	–	–	–	0	0	0	0
Timer 3 Counter Register	T3CNT	C4H	R	0	0	0	0	0	0	0	0
Reserved		C5H	–								
Timer 3 Data Register	T3DR	C6H	R/W	1	1	1	1	1	1	1	1
Timer 3 Capture Data Register	T3CDR	C6H	R	0	0	0	0	0	0	0	0
Reserved		C7H	–								
Timer 4 Control Low Register	T4CRL	C8H	R/W	0	0	0	0	0	0	0	0
Timer 4 Control High Register	T4CRH	C9H	R/W	0	–	0	0	–	–	0	0
Timer 1 Control Register	T1CR	CAH	R/W	0	0	0	0	0	0	0	0
Timer 1 Counter Register	T1CNT	CBH	R	0	0	0	0	0	0	0	0
Timer 1 Data Low Register	T1DRL	CCH	R/W	1	1	1	1	1	1	1	1
Timer 1 Data High Register	T1DRH	CDH	R/W	1	1	1	1	1	1	1	1
Timer 1 Capture Data Register	T1CDR	CDH	R	0	0	0	0	0	0	0	0
Carrier Mode Control Register	CARCR	CEH	R/W	–	–	0	0	–	–	0	0
Reserved		CFH	–								
Program Status Word Register	PSW	D0H	R/W	0	0	0	0	0	0	0	0
Reserved		D1H	–								
Timer 4 A Data Low Register	T4ADRL	D2H	R/W	1	1	1	1	1	1	1	1
Timer 4 A Data High Register	T4ADRH	D3H	R/W	1	1	1	1	1	1	1	1
P0 Pull-up Resistor Selection Register	P0PU	D4H	R/W	–	–	–	–	0	0	0	0
P1 Pull-up Resistor Selection Register	P1PU	D5H	R/W	0	0	0	0	0	0	0	0
P2 Pull-up Resistor Selection Register	P2PU	D6H	R/W	0	0	0	0	0	0	0	0
P3 Pull-up Resistor Selection Register	P3PU	D7H	R/W	0	0	0	0	0	0	0	0
Low Voltage Reset Control Register	LVRCR	D8H	R/W	0	–	–	0	0	0	0	0
Oscillator Control Register	OSCCR	D9H	R/W	–	–	0	0	1	0	0	0
P4 Pull-up Resistor Selection Register	P4PU	DAH	R/W	0	0	0	0	0	0	0	0
P5 Pull-up Resistor Selection Register	P5PU	DBH	R/W	0	0	0	0	0	0	0	0
P6 Pull-up Resistor Selection Register	P6PU	DCH	R/W	–	–	–	0	0	0	0	0
Reserved		DDH	–								
Timer 4 B Data Low Register	T4BDRL	DEH	R/W	1	1	1	1	1	1	1	1
Timer 4 B Data High Register	T4BDRH	DFH	R/W	1	1	1	1	1	1	1	1

7.3.3 SFR MAP (CONCLUDED)

Register Name	Mnemonic	Address Hex	R/W	@ RESET							
Accumulator Register	ACC	E0H	R/W	0	0	0	0	0	0	0	0
Low Voltage Indicator Control Register	LVICR	E1H	R/W	–	–	0	0	0	0	0	0
UART Control Register 1	UARTCR1	E2H	R/W	–	–	0	0	0	0	0	–
UART Control Register 2	UARTCR2	E3H	R/W	0	0	0	0	0	0	0	0
UART Control Register 3	UARTCR3	E4H	R/W	–	0	–	–	–	0	0	0
UART Status Register	UARTST	E5H	R/W	1	0	0	0	0	0	0	0
UART Baud Rate Generation Register	UARTBD	E6H	R/W	1	1	1	1	1	1	1	1
UART Data Register	UARTDR	E7H	R/W	0	0	0	0	0	0	0	0
Key Interrupt Flag Register	KFLAG	E8H	R/W	0	0	0	0	0	0	0	0
P0 Debounce Enable Register	P0DB	E9H	R/W	0	0	–	–	–	0	0	0
P1 Debounce Enable Register	P1DB	EAH	R/W	0	0	0	0	0	0	0	0
LCD Driver Control Low Register	LCDCRL	EBH	R/W	0	0	0	0	0	0	0	0
LCD Driver Control High Register	LCDCRH	ECH	R/W	–	–	–	–	–	–	–	0
Port 0 Function Selection Register	P0FSR	EDH	R/W	0	0	0	0	0	0	0	0
Port 2 Function Selection Register	P2FSR	EEH	R/W	0	0	0	0	0	0	0	0
Port 3 Function Selection Register	P3FSR	EFH	R/W	0	0	0	0	0	0	0	0
B Register	B	F0H	R/W	0	0	0	0	0	0	0	0
Port 4 Function Selection Register	P4FSR	F1H	R/W	0	0	0	0	0	0	0	0
Port 5 Function Selection Low Register	P5FSRL	F2H	R/W	–	–	–	–	0	0	0	0
Port 5 Function Selection High Register	P5FSRH	F3H	R/W	–	0	0	0	0	0	0	0
Port 6 Function Selection Register	P6FSR	F4H	R/W	–	–	–	0	0	0	0	0
LCD Contrast Control Register	LCDCCR	F5H	R/W	0	–	–	–	0	0	0	0
Port 1 Function Selection Low Register	P1FSRL	F6H	R/W	–	0	0	0	0	0	0	0
Port 1 Function Selection High Register	P1FSRH	F7H	R/W	–	–	–	–	0	0	0	0
Interrupt Priority Register 1	IP1	F8H	R/W	–	–	0	0	0	0	0	0
Reserved		F9H	–								
Flash Sector Address High Register	FSADRH	FAH	R/W	–	–	–	–	0	0	0	0
Flash Sector Address Middle Register	FSADRM	FBH	R/W	0	0	0	0	0	0	0	0
Flash Sector Address Low Register	FSADRL	FCH	R/W	0	0	0	0	0	0	0	0
Flash Identification Register	FIDR	FDH	R/W	0	0	0	0	0	0	0	0
Flash Mode Control Register	FMCR	FEH	R/W	0	–	–	–	–	0	0	0
Phase Locked Loop Control Register	PLLCR	FFH	R/W	–	–	0	0	0	0	0	0

7.3.4 COMPILER COMPATIBLE SFR

ACC (Accumulator Register) : E0H

.7	.6	.5	.4	.3	.2	.1	.0
ACC							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

ACC Accumulator

B (B Register) : F0H

.7	.6	.5	.4	.3	.2	.1	.0
B							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

B B Register

SP (Stack Pointer) : 81H

.7	.6	.5	.4	.3	.2	.1	.0
SP							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 07H

SP Stack Pointer

DPL (Data Pointer Register Low) : 82H

.7	.6	.5	.4	.3	.2	.1	.0
DPL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPL Data Pointer Low Byte

DPH (Data Pointer Register High) : 83H

.7	.6	.5	.4	.3	.2	.1	.0
DPH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPH Data Pointer High Byte

DPL1 (Data Pointer Register Low 1) : 84H

.7	.6	.5	.4	.3	.2	.1	.0
DPL1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPL1 Data Pointer Low 1 Byte

DPH1 (Data Pointer Register High 1) : 85H

.7	.6	.5	.4	.3	.2	.1	.0
DPH1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPH1 Data Pointer High 1 Byte

PSW (Program Status Word) : D0H

.7	.6	.5	.4	.3	.2	.1	.0
CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

CY Carry Flag

AC Auxiliary Carry Flag

F0 General Purpose User-Definable Flag

RS1 Register Bank Select bit 1

RS0 Register Bank Select bit 0

OV Overflow Flag

F1 User-Definable Flag

P Parity Flag. Set/Clear by hardware each instruction cycle to indicate an odd/even number of ‘1’bits in the accumulator.

EO (Extended Operation Register) : A2H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	TRAP_EN	–	DPSEL2	DPSEL1	DPSEL0
–	–	–	R/W	–	R/W	R/W	R/W

Initial value: 00H

TRAP_EN Select the Instruction (Keep always ‘0’)

0 Select MOVC @(DPTR++), A

1 Select Software TRAP Instruction

DPSEL[2:0] Select Banked Data Pointer Register

DPSEL2	DPSEL1	DPSEL0	description
0	0	0	DPTR0
0	0	1	DPTR1
Reserved			

8. I/O Ports

8.1 PORT REGISTER

8.1.1 REGISTER MAP

Name	Address	Dir	Default	Description
P0	80H	R/W	00H	P0 Data Register
P0IO	89H	R/W	00H	P0 Direction Register
P0PU	D4H	R/W	00H	P0 Pull-up Resistor Selection Register
P0OD	92H	R/W	00H	P0 Open-drain Selection Register
P0DB	E9H	R/W	00H	P0 Debounce Enable Register
P0FSR	EDH	R/W	00H	Port 0 Function Selection Register
P1	88H	R/W	00H	P1 Data Register
P1IO	91H	R/W	00H	P1 Direction Register
P1PU	D5H	R/W	00H	P1 Pull-up Resistor Selection Register
P1OD	93H	R/W	00H	P1 Open-drain Selection Register
P1DB	EAH	R/W	00H	P1 Debounce Enable Register
P1FSRH	F7H	R/W	00H	Port 1 Function Selection High Register
P1FSRL	F6H	R/W	00H	Port 1 Function Selection Low Register
P2	90H	R/W	00H	P2 Data Register
P2IO	99H	R/W	00H	P2 Direction Register
P2PU	D6H	R/W	00H	P2 Pull-up Resistor Selection Register
P2OD	94H	R/W	00H	P2 Open-drain Selection Register
P2FSR	EEH	R/W	00H	Port 2 Function Selection Register
P3	98H	R/W	00H	P3 Data Register
P3IO	A1H	R/W	00H	P3 Direction Register
P3PU	D7H	R/W	00H	P3 Pull-up Resistor Selection Register
P3OD	95H	R/W	00H	P3 Open-drain Selection Register
P3FSR	EFH	R/W	00H	Port 3 Function Selection Register
P4	A0H	R/W	00H	P4 Data Register
P4IO	B1H	R/W	00H	P4 Direction Register
P4PU	DAH	R/W	00H	P4 Pull-up Resistor Selection Register
P4OD	96H	R/W	00H	P4 Open-drain Selection Register
P4FSR	F1H	R/W	00H	Port 4 Function Selection Register

Table 8-1 Register Map

8.1.1 REGISTER MAP (CONCLUDED)

Name	Address	Dir	Default	Description
P5	B0H	R/W	00H	P5 Data Register
P5IO	B9H	R/W	00H	P5 Direction Register
P5PU	DBH	R/W	00H	P5 Pull-up Resistor Selection Register
P5OD	9AH	R/W	00H	P5 Open-drain Selection Register
P5FSRH	F3H	R/W	00H	Port 5 Function Selection High Register
P5FSRL	F2H	R/W	00H	Port 5 Function Selection Low Register
P6	C0H	R/W	00H	P6 Data Register
P6IO	C1H	R/W	00H	P6 Direction Register
P6PU	DCH	R/W	00H	P6 Pull-up Resistor Selection Register
P6OD	9BH	R/W	00H	P6 Open-drain Selection Register
P6FSR	F4H	R/W	00H	Port 6 Function Selection Register

Table 8-1 Register Map

8.2 P0 PORT

8.2.1 REGISTER DESCRIPTION FOR P0

P0 (P0 Data Register) : 80H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	P03	P02	P01	P00
–	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

P0[3:0] I/O Data

P0IO (P0 Direction Register) : 89H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	P03IO	P02IO	P01IO	P00IO
–	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

P0IO[3:0] P0 Data I/O Direction

0 Input

1 Output

Note: EINT10/EINT12/**EINT14**/EC2 function possible when input

P0PU (P0 Pull-up Resistor Selection Register) : D4H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	P03PU	P02PU	P01PU	P00PU
–	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

P0PU[3:0] Configure Pull-up Resistor of P0 Port

0 Disable

1 Enable

P0OD (P0 Open-drain Selection Register) : 92H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	P03OD	P02OD	P01OD	P00OD
–	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

P0OD[3:0] Configure Open-drain of P0 Port

0 Disable

1 Enable

P0DB (P0 Debounce Enable Register) : E9H

.7	.6	.5	.4	.3	.2	.1	.0
DBCLK1	DBCLK0	–	–	–	P02DB	P01DB	P00DB
R/W	R/W	–	–	–	R/W	R/W	R/W

Initial value: 00H

DBCLK[1:0] Configure Debounce Clock of Port

DBCLK1	DBCLK0	description
0	0	fx (SCLK)
0	1	fxx/4
1	0	fxx/4096
0	1	Reserved

P02DB Configure Debounce of P02

0 Disable

1 Enable

P01DB Configure Debounce of P01

0 Disable

1 Enable

P00DB Configure Debounce of P00

0 Disable

1 Enable

Notes:

1. If a level is not detected on an enabled pin three or four times in a row at the sampling clock, the signal is eliminated as noise.
2. A pulse level should be input for the duration of 3 clocks or more to be actually detected as a valid edge.
3. The port debounce is automatically disabled at stop mode and recovered after stop mode release.

P0FSR (Port 0 Function Selection Register) : EDH

.7	.6	.5	.4	.3	.2	.1	.0
P0FSR7	P0FSR6	P0FSR5	P0FSR4	P0FSR3	P0FSR2	P0FSR1	P0FSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P0FSR[7:6] P03 Function Select

P0FSR7	P0FSR6	Description
0	0	I/O Port
0	1	REM Function
1	0	SEG33 Function
1	1	Not used

P0FSR[5:4] P02 Function Select

P0FSR5	P0FSR4	Description
0	0	I/O Port (EINT14 function possible if the P02 is an input and the P10 is not selected as EINT14 function)
0	1	BUZO Function
1	0	SEG32 Function
1	1	EC4 Function

P0FSR[3:2] P01 Function Select

P0FSR3	P0FSR2	Description
0	0	I/O Port (EINT12/EC2 function possible when input)
0	1	T2O Function
1	0	SEG31 Function
1	1	Not used

P0FSR[1:0] P00 Function Select

P0FSR1	P0FSR0	Description
0	0	I/O Port (EINT10 function possible when input)
0	1	T4O/PWM4O Function
1	0	SEG30 Function
1	1	Not used

8.3 P1 PORT

8.3.1 REGISTER DESCRIPTION FOR P1

P1 (P1 Data Register) : 88H

.7	.6	.5	.4	.3	.2	.1	.0
P17	P16	P15	P14	P13	P12	P11	P10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P1[7:0] I/O Data

P1IO (P1 Direction Register) : 91H

.7	.6	.5	.4	.3	.2	.1	.0
P17IO	P16IO	P15IO	P14IO	P13IO	P12IO	P11IO	P10IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P1IO[7:0] P1 Data I/O Direction

0 Input

1 Output

Note: KEY0 – KEY7 function possible when input

P1PU (P1 Pull-up Resistor Selection Register) : D5H

.7	.6	.5	.4	.3	.2	.1	.0
P17PU	P16PU	P15PU	P14PU	P13PU	P12PU	P11PU	P10PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P1PU[7:0] Configure Pull-up Resistor of P1 Port

0 Disable

1 Enable

P1OD (P1 Open-drain Selection Register) : 93H

.7	.6	.5	.4	.3	.2	.1	.0
P17OD	P16OD	P15OD	P14OD	P13OD	P12OD	P11OD	P10OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P1OD[7:0] Configure Open-drain of P1 Port

0 Disable

1 Enable

P1DB (P1 Debounce Enable Register) : EAH

.7	.6	.5	.4	.3	.2	.1	.0
P17DB	P16DB	P15DB	P14DB	P13DB	P12DB	P11DB	P10DB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P1DB[7:0] Configure Debounce of P1 Port

0 Disable

1 Enable

Notes:

1. If a level is not detected on an enabled pin three or four times in a row at the sampling clock, the signal is eliminated as noise.
2. A pulse level should be input for the duration of 3 clocks or more to be actually detected as a valid edge.
3. The port debounce is automatically disabled at stop mode and recovered after stop mode release.
4. Refer to the Port 0 debounce enable register (P0DB) for the debounce clock of port 1.

P1FSRH (Port 1 Function Selection High Register) : F7H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	P1FSRH3	P1FSRH2	P1FSRH1	P1FSRH0
–	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

P1FSRH3 P17 Function Select

0 I/O Port (KEY7 function possible when input)

1 AN7 Function

P1FSRH2 P16 Function Select

0 I/O Port (KEY6 function possible when input)

1 AN6 Function

P1FSRH1 P15 Function Select

0 I/O Port (KEY5 function possible when input)

1 AN5 Function

P1FSRH0 P14 Function Select

0 I/O Port (KEY4 function possible when input)

1 AN4 Function

P1FSRL (Port 1 Function Selection Low Register) : F6H

.7	.6	.5	.4	.3	.2	.1	.0
–	P1FSRL6	P1FSRL5	P1FSRL4	P1FSRL3	P1FSRL2	P1FSRL1	P1FSRL0
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P1FSRL6 P13 Function Select

0 I/O Port (KEY3 function possible when input)

1 AN3 Function

P1FSRL[5:4] P12 Function Select

P1FSRL5	P1FSRL4	Description
0	0	I/O Port (KEY2 function possible when input)
0	1	AN2 Function
1	0	BUZO Function
1	1	EC4 Function

P1FSRL[3:2] P11 Function Select

P1FSRL3	P1FSRL2	Description
0	0	I/O Port (KEY1 function possible when input)
0	1	AN1 Function
1	0	REM Function
1	1	Not used

P1FSRL[1:0] P10 Function Select

P1FSRL1	P1FSRL0	Description
0	0	I/O Port (KEY0 function possible when input)
0	1	AN0 Function
1	0	T4O/PWM4O Function
1	1	EINT14 Function

8.4 P2 PORT

8.4.1 REGISTER DESCRIPTION FOR P2

P2 (P2 Data Register) : 90H

.7	.6	.5	.4	.3	.2	.1	.0
P27	P26	P25	P24	P23	P22	P21	P20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P2[7:0] I/O Data

P2IO (P2 Direction Register) : 99H

.7	.6	.5	.4	.3	.2	.1	.0
P27IO	P26IO	P25IO	P24IO	P23IO	P22IO	P21IO	P20IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P2IO[7:0] P2 Data I/O Direction

0 Input

1 Output

P2PU (P2 Pull-up Resistor Selection Register) : D6H

.7	.6	.5	.4	.3	.2	.1	.0
P27PU	P26PU	P25PU	P24PU	P23PU	P22PU	P21PU	P20PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P2PU[7:0] Configure Pull-up Resistor of P2 Port

0 Disable

1 Enable

P2OD (P2 Open-drain Selection Register) : 94H

.7	.6	.5	.4	.3	.2	.1	.0
P27OD	P26OD	P25OD	P24OD	P23OD	P22OD	P21OD	P20OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P2OD[7:0] Configure Open-drain of P2 Port

0 Disable

1 Enable

P2FSR (Port 2 Function Selection Register) : EEH

.7	.6	.5	.4	.3	.2	.1	.0
P2FSR7	P2FSR6	P2FSR5	P2FSR4	P2FSR3	P2FSR2	P2FSR1	P2FSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P2FSR7 P27 Function Select
- 0 I/O Port
- 1 COM7/SEG5 Function

P2FSR6 P26 Function Select
- 0 I/O Port
- 1 COM6/SEG4 Function

P2FSR5 P25 Function Select
- 0 I/O Port
- 1 COM5/SEG3 Function

P2FSR4 P24 Function Select
- 0 I/O Port
- 1 COM4/SEG2 Function

P2FSR3 P23 Function Select
- 0 I/O Port
- 1 COM3/SEG1 Function

P2FSR2 P22 Function Select
- 0 I/O Port
- 1 COM2/SEG0 Function

P2FSR1 P21 Function Select
- 0 I/O Port
- 1 COM1 Function

P2FSR0 P20 Function Select
- 0 I/O Port
- 1 COM0 Function

Note: The P22-P27 is automatically configured as common or segment signal according to the duty in the LCDCRL register when the pin is selected as the sub-function for common/segment.

8.5 P3 PORT

8.5.1 REGISTER DESCRIPTION FOR P3

P3 (P3 Data Register) : 98H

.7	.6	.5	.4	.3	.2	.1	.0
P37	P36	P35	P34	P33	P32	P31	P30
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P3[7:0] I/O Data

P3IO (P3 Direction Register) : A1H

.7	.6	.5	.4	.3	.2	.1	.0
P37IO	P36IO	P35IO	P34IO	P33IO	P32IO	P31IO	P30IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P3IO[7:0] P3 Data I/O Direction

0 Input

1 Output

P3PU (P3 Pull-up Resistor Selection Register) : D7H

.7	.6	.5	.4	.3	.2	.1	.0
P37PU	P36PU	P35PU	P34PU	P33PU	P32PU	P31PU	P30PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P3PU[7:0] Configure Pull-up Resistor of P3 Port

0 Disable

1 Enable

P3OD (P3 Open-drain Selection Register) : 95H

.7	.6	.5	.4	.3	.2	.1	.0
P37OD	P36OD	P35OD	P34OD	P33OD	P32OD	P31OD	P30OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P3OD[7:0] Configure Open-drain of P3 Port

0 Disable

1 Enable

P3FSR (Port 3 Function Selection Register) : EFH

.7	.6	.5	.4	.3	.2	.1	.0
P3FSR7	P3FSR6	P3FSR5	P3FSR4	P3FSR3	P3FSR2	P3FSR1	P3FSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P3FSR7 P37 Function Select
- 0 I/O Port
- 1 SEG13 Function

P3FSR6 P36 Function Select
- 0 I/O Port
- 1 SEG12 Function

P3FSR5 P35 Function Select
- 0 I/O Port
- 1 SEG11 Function

P3FSR4 P34 Function Select
- 0 I/O Port
- 1 SEG10 Function

P3FSR3 P33 Function Select
- 0 I/O Port
- 1 SEG9 Function

P3FSR2 P32 Function Select
- 0 I/O Port
- 1 SEG8 Function

P3FSR1 P31 Function Select
- 0 I/O Port
- 1 SEG7 Function

P3FSR0 P30 Function Select
- 0 I/O Port
- 1 SEG6 Function

8.6 P4 PORT

8.6.1 REGISTER DESCRIPTION FOR P4

P4 (P4 Data Register) : A0H

.7	.6	.5	.4	.3	.2	.1	.0
P47	P46	P45	P44	P43	P42	P41	P40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P4[7:0] I/O Data

P4IO (P4 Direction Register) : B1H

.7	.6	.5	.4	.3	.2	.1	.0
P47IO	P46IO	P45IO	P44IO	P43IO	P42IO	P41IO	P40IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P4IO[7:0] P4 Data I/O Direction

0 Input

1 Output

P4PU (P4 Pull-up Resistor Selection Register) : DAH

.7	.6	.5	.4	.3	.2	.1	.0
P47PU	P46PU	P45PU	P44PU	P43PU	P42PU	P41PU	P40PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P4PU[7:0] Configure Pull-up Resistor of P4 Port

0 Disable

1 Enable

P4OD (P4 Open-drain Selection Register) : 96H

.7	.6	.5	.4	.3	.2	.1	.0
P47OD	P46OD	P45OD	P44OD	P43OD	P42OD	P41OD	P40OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P4OD[7:0] Configure Open-drain of P4 Port

0 Disable

1 Enable

P4FSR (Port 4 Function Selection Register) : F1H

.7	.6	.5	.4	.3	.2	.1	.0
P4FSR7	P4FSR6	P4FSR5	P4FSR4	P4FSR3	P4FSR2	P4FSR1	P4FSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P4FSR7 P47 Function Select
- 0 I/O Port
- 1 SEG21 Function

P4FSR6 P46 Function Select
- 0 I/O Port
- 1 SEG20 Function

P4FSR5 P45 Function Select
- 0 I/O Port
- 1 SEG19 Function

P4FSR4 P44 Function Select
- 0 I/O Port
- 1 SEG18 Function

P4FSR3 P43 Function Select
- 0 I/O Port
- 1 SEG17 Function

P4FSR2 P42 Function Select
- 0 I/O Port
- 1 SEG16 Function

P4FSR1 P41 Function Select
- 0 I/O Port
- 1 SEG15 Function

P4FSR0 P40 Function Select
- 0 I/O Port
- 1 SEG14 Function

8.7 P5 PORT

8.7.1 REGISTER DESCRIPTION FOR P5

P5 (P5 Data Register) : B0H

.7	.6	.5	.4	.3	.2	.1	.0
P57	P56	P55	P54	P53	P52	P51	P50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P5[7:0] I/O Data

P5IO (P5 Direction Register) : B9H

.7	.6	.5	.4	.3	.2	.1	.0
P57IO	P56IO	P55IO	P54IO	P53IO	P52IO	P51IO	P50IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P5IO[7:0] P5 Data I/O Direction

0 Input

1 Output

Note: EC0/SI/SCK-in/RXD function possible when input

P5PU (P5 Pull-up Resistor Selection Register) : DBH

.7	.6	.5	.4	.3	.2	.1	.0
P57PU	P56PU	P55PU	P54PU	P53PU	P52PU	P51PU	P50PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P5PU[7:0] Configure Pull-up Resistor of P5 Port

0 Disable

1 Enable

P5OD (P5 Open-drain Selection Register) : 9AH

.7	.6	.5	.4	.3	.2	.1	.0
P57OD	P56OD	P55OD	P54OD	P53OD	P52OD	P51OD	P50OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P5OD[7:0] Configure Open-drain of P5 Port

0 Disable

1 Enable

P5FSRH (Port 5 Function Selection High Register) : F3H

.7	.6	.5	.4	.3	.2	.1	.0
–	P5FSRH6	P5FSRH5	P5FSRH4	P5FSRH3	P5FSRH2	P5FSRH1	P5FSRH0
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P5FSRH[6:5] P57 Function Select

P5FSRH6	P5FSRH5	Description
0	0	I/O Port (RXD function possible when input)
0	1	SO Function
1	0	SEG29 Function
1	1	Not used

P5FSRH[4:3] P56 Function Select

P5FSRH4	P5FSRH3	Description
0	0	I/O Port (SCK-in function possible when input)
0	1	SCK-out Function
1	0	SEG28 Function
1	1	TXD Function

P5FSRH2 P55 Function Select

0	I/O Port (SI function possible when input)
1	SEG27

P5FSRH[1:0] P54 Function Select

P5FSRH1	P5FSRH0	Description
0	0	I/O Port (EC0 function possible when input)
0	1	T0O Function
1	0	SEG26 Function
1	1	Not used

P5FSRL (Port 5 Function Selection Low Register) : F2H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	P5FSRL3	P5FSRL2	P5FSRL1	P5FSRL0
–	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

P5FSRL3 P53 Function Select
- 0 I/O Port
- 1 SEG25 Function

P5FSRL2 P52 Function Select
- 0 I/O Port
- 1 SEG24 Function

P5FSRL1 P51 Function Select
- 0 I/O Port
- 1 SEG23 Function

P5FSRL0 P50 Function Select
- 0 I/O Port
- 1 SEG22 Function

8.8 P6 PORT

8.8.1 REGISTER DESCRIPTION FOR P6

P6 (P6 Data Register) : C0H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	P64	P63	P62	P61	P60
–	–	–	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P6[4:0] I/O Data

P6IO (P6 Direction Register) : C1H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	P64IO	P63IO	P62IO	P61IO	P60IO
–	–	–	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P6IO[4:0] P6 Data I/O Direction

0 Input

1 Output

P6PU (P6 Pull-up Resistor Selection Register) : DCH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	P64PU	P63PU	P62PU	P61PU	P60PU
–	–	–	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P6PU[4:0] Configure Pull-up Resistor of P6 Port

0 Disable

1 Enable

P6OD (P6 Open-drain Selection Register) : 9BH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	P64OD	P63OD	P62OD	P61OD	P60OD
–	–	–	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

P6OD[4:0] Configure Open-drain of P6 Port

0 Disable

1 Enable

P6FSR (Port 6 Function Selection Register) : F4H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	P6FSR3	P6FSR2	P6FSR1	P6FSR0
–	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

P6FSR3 P64 Function Select
- 0 I/O Port
- 1 SXOUT Function

P6FSR2 P63 Function Select
- 0 I/O Port
- 1 SXIN Function

P6FSR1 P61 Function Select
- 0 I/O Port
- 1 XIN Function

P6FSR0 P60 Function Select
- 0 I/O Port
- 1 XOUT Function

Notes: 1. The pull-up resistor of P60/P61/P63/P64 is automatically disabled regardless of the corresponding pull-up resistor enable bit if the P60/P61/P63/P64 is configured as an x-tal function (XIN/XOUT/SXIN/SXOUT).
2. The P6FSR[1:0]/P6FSR[3:2] bits are not changed during f_{XIN}/f_{SUB} is selected as the system clock (fx).
3. Refer to the configure option for the P62/RESETB.

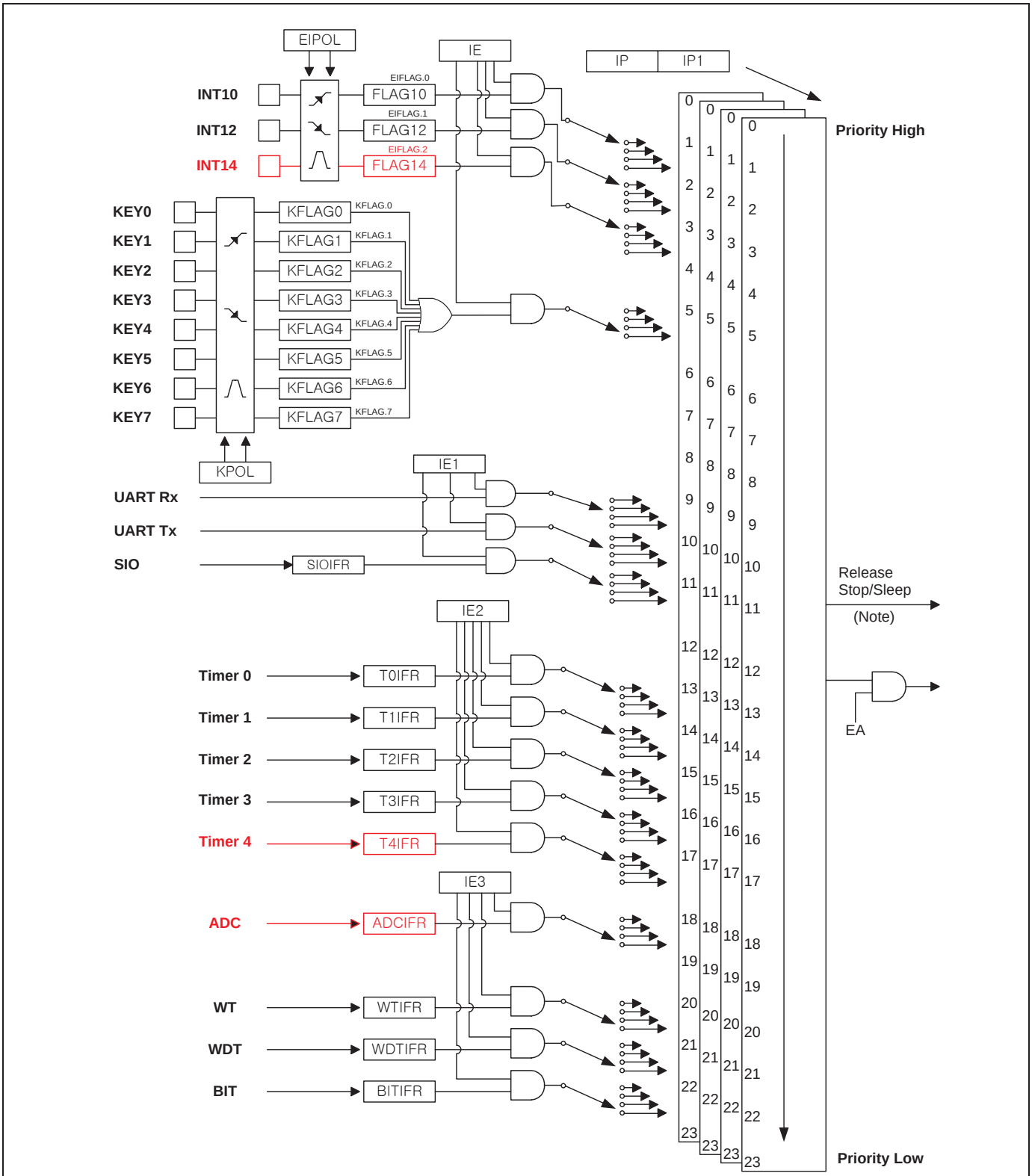
9. Interrupt Controller

9.1 INTERRUPT GROUP PRIORITY LEVEL

Interrupt Group	Highest → Lowest				
0 (Bit0)	Interrupt 0	Interrupt 6	Interrupt 12	Interrupt 18	Highest
1 (Bit1)	Interrupt 1	Interrupt 7	Interrupt 13	Interrupt 19	
2 (Bit2)	Interrupt 2	Interrupt 8	Interrupt 14	Interrupt 20	
3 (Bit3)	Interrupt 3	Interrupt 9	Interrupt 15	Interrupt 21	
4 (Bit4)	Interrupt 4	Interrupt 10	Interrupt 16	Interrupt 22	
5 (Bit5)	Interrupt 5	Interrupt 11	Interrupt 17	Interrupt 23	Lowest

Interrupt Group Priority Level

9.2 INTERRUPT BLOCK DIAGRAM



Notes: 1. The release signal may be generated by all interrupt sources which are enabled without reference to a priority level.
2. An interrupt request is delayed during data are written to IE, IE1, IE2, IE3, IP, IP1, and PCON register.

9.3 INTERRUPT VECTOR TABLE

Interrupt Source	Symbol	Interrupt Enable Bit	Priority	Mask	Vector Address
Hardware RESET	RESETB	0 0	0	Non-Maskable	0000H
-	INT0	IE.0	1	Maskable	0003H
External Interrupt 10	INT1	IE.1	2	Maskable	000BH
External Interrupt 12	INT2	IE.2	3	Maskable	0013H
External Interrupt 14	INT3	IE.3	4	Maskable	001BH
-	INT4	IE.4	5	Maskable	0023H
KEY Interrupt	INT5	IE.5	6	Maskable	002BH
-	INT6	IE1.0	7	Maskable	0033H
-	INT7	IE1.1	8	Maskable	003BH
-	INT8	IE1.2	9	Maskable	0043H
UART Rx Interrupt	INT9	IE1.3	10	Maskable	004BH
UART Tx Interrupt	INT10	IE1.4	11	Maskable	0053H
SIO Interrupt	INT11	IE1.5	12	Maskable	005BH
-	INT12	IE2.0	13	Maskable	0063H
T0 Interrupt	INT13	IE2.1	14	Maskable	006BH
T1 Interrupt	INT14	IE2.2	15	Maskable	0073H
T2 Interrupt	INT15	IE2.3	16	Maskable	007BH
T3 Interrupt	INT16	IE2.4	17	Maskable	0083H
T4 Interrupt	INT17	IE2.5	18	Maskable	008BH
ADC Interrupt	INT18	IE3.0	19	Maskable	0093H
-	INT19	IE3.1	20	Maskable	009BH
WT Interrupt	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
-	INT23	IE3.5	24	Maskable	00BBH

9.3.1 REGISTER MAP

Name	Address	Dir	Default	Description
IE	A8H	R/W	00H	Interrupt Enable Register
IE1	A9H	R/W	00H	Interrupt Enable Register 1
IE2	AAH	R/W	00H	Interrupt Enable Register 2
IE3	ABH	R/W	00H	Interrupt Enable Register 3
IP	B8H	R/W	00H	Interrupt Priority Register
IP1	F8H	R/W	00H	Interrupt Priority Register 1
EIFLAG	A4H	R/W	00H	External Interrupt Flag Register
EIPOL	A5H	R/W	00H	External Interrupt Polarity Register
KFLAG	E8H	R/W	00H	KEY Interrupt Flag Register
KPOL1	AFH	R/W	00H	KEY Interrupt Polarity 1 Register
KPOL0	AEH	R/W	00H	KEY Interrupt Polarity 0 Register

Register Map

9.3.2 REGISTER DESCRIPTION FOR INTERRUPT

IE (Interrupt Enable Register) : A8H

.7	.6	.5	.4	.3	.2	.1	.0
EA	–	INT5E	–	INT3E	INT2E	INT1E	–
R/W	–	R/W	–	R/W	R/W	R/W	–

Initial value: 00H

EA Enable or disable all interrupt bits
- 0 All interrupt disable
- 1 All interrupt enable

INT5E Enable or disable Key interrupt (KEY0 – KEY7)
- 0 Disable
- 1 Enable

INT3E Enable or disable External interrupt 14 (EINT14)
- 0 Disable
- 1 Enable

INT2E Enable or disable External interrupt 12 (EINT12)
- 0 Disable
- 1 Enable

INT1E Enable or disable External interrupt 10 (EINT10)
- 0 Disable
- 1 Enable

IE1 (Interrupt Enable Register 1) : A9H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	INT11E	INT10E	INT9E	–	–	–
–	–	R/W	R/W	R/W	–	–	–

Initial value: 00H

INT11E Enable or disable SIO interrupt
- 0 Disable
- 1 Enable

INT10E Enable or disable UART Tx interrupt
- 0 Disable
- 1 Enable

INT9E Enable or disable UART Rx interrupt
- 0 Disable
- 1 Enable

IE2 (Interrupt Enable Register 2) : AAH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	INT17E	INT16E	INT15E	INT14E	INT13E	–
–	–	R/W	R/W	R/W	R/W	R/W	–

Initial value: 00H

INT17E Enable or disable Timer 4 interrupt
0 Disable
1 Enable

INT16E Enable or disable Timer 3 interrupt
0 Disable
1 Enable

INT15E Enable or disable Timer 2 interrupt
0 Disable
1 Enable

INT14E Enable or disable Timer 1 interrupt
0 Disable
1 Enable

INT13E Enable or disable Timer 0 interrupt
0 Disable
1 Enable

IE3 (Interrupt Enable Register 3) : ABH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	INT22E	INT21E	INT20E	–	INT18E
–	–	–	R/W	R/W	R/W	–	R/W

Initial value: 00H

INT22E Enable or disable BIT interrupt

0 Disable

1 Enable

INT21E Enable or disable WDT interrupt

0 Disable

1 Enable

INT20E Enable or disable WT interrupt

0 Disable

1 Enable

INT18E Enable or disable ADC interrupt

0 Disable

1 Enable

IP (Interrupt Priority Register) : B8H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	IP5	IP4	IP3	IP2	IP1	IP0
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

IP1 (Interrupt Priority Register 1) : F8H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	IP15	IP14	IP13	IP12	IP11	IP10
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

IP[5:0], IP1[5:0] Select Interrupt Group Priority

IP1x	IPx	Description
0	0	level 0 (lowest)
0	1	level 1
1	0	level 2
1	1	level 3 (highest)

EIFLAG (External Interrupt Flag Register) : A4H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	–	FLAG14	FLAG12	FLAG10
–	–	–	–	–	R/W	R/W	R/W

Initial value: 00H

FLAG[2:0] When an external interrupt is occurred, the flag becomes ‘1’. The flag is cleared by writing ‘0’ to the bit or automatically cleared by INT_ACK signal. Writing “1” has no effect.

0	External Interrupt not occurred
1	External Interrupt occurred

EIPOL (External Interrupt Polarity Register) : A5H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	POL14		POL12		POL10	
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

POL[5:0] External interrupt (EINT10/EINT12/EINT14) polarity selection

POLn[1:0]		Description
0	0	No interrupt at any edge
0	1	Interrupt on rising edge
1	0	Interrupt on falling edge
1	1	Interrupt on both of rising and falling edge

Where n = 10, 12, and 14

KFLAG (Key Interrupt Flag Register) : E8H

.7	.6	.5	.4	.3	.2	.1	.0
KFLAG7	KFLAG6	KFLAG5	KFLAG4	KFLAG3	KFLAG2	KFLAG1	KFLAG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

KFLAG[7:0] When Key interrupt is occurred, the flag becomes ‘1’.
The flag is cleared only by writing ‘0’ to the bit. So, the flag should be cleared by software. Writing “1” has no effect.

0	Key Interrupt 0 ~ 7 not occurred
1	Key Interrupt 0 ~ 7occurred

KPOL1 (Key Interrupt Polarity 1 Register) : AFH

.7	.6	.5	.4	.3	.2	.1	.0
KPOL7		KPOL6		KPOL5		KPOL4	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

KPOL1[7:0] Key interrupt (KEY4,,,,,,, KEY7) polarity selection

KPOL1n[1:0]		Description
0	0	No interrupt at any edge
0	1	Interrupt on rising edge
1	0	Interrupt on falling edge
1	1	Interrupt on both of rising and falling edge

Where n = 4, 5, 6, and 7

KPOL0 (Key Interrupt Polarity 0 Register) : AEH

.7	.6	.5	.4	.3	.2	.1	.0
KPOL3		KPOL2		KPOL1		KPOL0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

KPOL0[7:0] Key interrupt (KEY0,,,,,,, KEY3) polarity selection

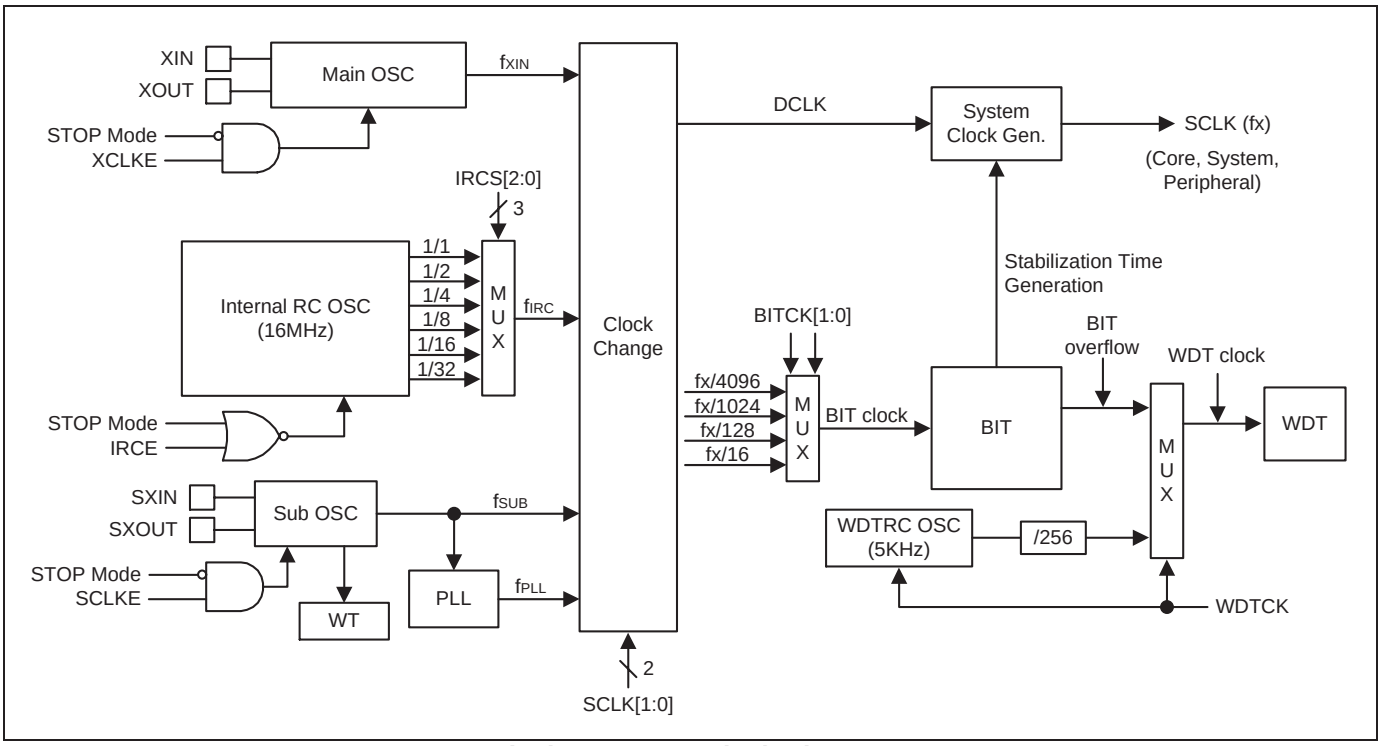
KPOL0n[1:0]		Description
0	0	No interrupt at any edge
0	1	Interrupt on rising edge
1	0	Interrupt on falling edge
1	1	Interrupt on both of rising and falling edge

Where n = 0, 1, 2, and 3

10. Peripheral Hardware

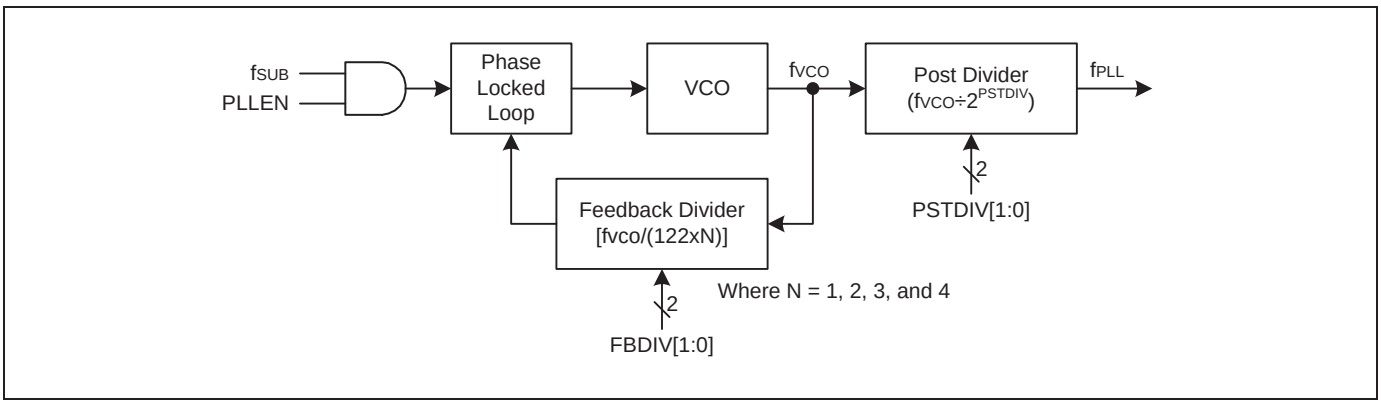
10.1 CLOCK GENERATOR

10.1.1 BLOCK DIAGRAM



Clock Generator Block Diagram

10.1.2 PLL CIRCUIT DIAGRAM



PLL Circuit Diagram

10.1.3 REGISTER MAP

Name	Address	Dir	Default	Description
SCCR	8AH	R/W	00H	System and Clock Control Register
OSCCR	D9H	R/W	08H	Oscillator Control Register
PLLCR	FFH	R/W	00H	Phase Locked-Loop Control Register

Register Map

10.1.4 REGISTER DESCRIPTION CLOCK GENERATOR

SCCR (System and Clock Control Register) : 8AH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	–	–	SCLK1	SCLK0
–	–	–	–	–	–	R/W	R/W

Initial value: 00H

SCLK[1:0] System Clock Selection Bit

SCLK1	SCLK0	Description
0	0	INT-RC OSC (f_{IRC}) for system clock
0	1	External Main OSC (f_{XIN}) for system clock
1	0	External Sub OSC (f_{SUB}) for system clock
1	1	Phase Locked-Loop (f_{PLL}) for system clock

Note: If a target system clock is disabled by the OSCCR register, the SCCR register won't be changed in case of selecting the corresponding clock as a system clock.

OSCCR (Oscillator Control Register) : D9H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	IRCS2	IRCS1	IRCS0	IRCE	XCLKE	SCLKE
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 08H

IRCS[2:0] Internal RC oscillator post-divider selection

IRCS2	IRCS1	IRCS0	Description
0	0	0	f_{IRC}/32 (0.5MHz)
0	0	1	f_{IRC}/16 (1MHz)
0	1	0	f_{IRC}/8 (2MHz)
0	1	1	f_{IRC}/4 (4MHz)
1	0	0	f_{IRC}/2 (8MHz)
1	0	1	f_{IRC}/1 (16MHz)
Other values			Not used

IRCE Control the operation of the internal RC oscillator

0 Enable operation of INT-RC OSC

1 Disable operation of INT-RC OSC

XCLKE Control the operation of the external main oscillator

0 Disable operation of X-TAL

1 Enable operation of X-TAL

SCLKE Control the operation of the external sub oscillator

0 Disable operation of SX-TAL

1 Enable operation of SX-TAL

Note: The system clock is not disabled by the corresponding bit of the OSCCR register. Ex) The internal RC oscillator won't be disabled by the IRCE bit during the f_{IRC} is selected as the system clock**.**

PLLCR (Phase Locked Loop Control Register) : FFH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	PLLSTA	FBDIV1	FBDIV0	PSTDIV1	PSTDIV0	PLLEN
–	–	R	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

PLLSTA PLL Locked/Unlocked Status Bit

0 PLL currently in unlocked state

1 PLL currently in locked state

FBDIV[1:0] PLL Pre-Divider Selection Bits.

FBDIV1	FBDIV0	Description
0	0	f_{VCO} = 15.9908MHz
0	1	f_{VCO} = 11.9931MHz
1	0	f_{VCO} = 7.9954MHz
1	1	f_{VCO} = 3.9977MHz

PSTDIV[1:0] PLL Post-Divider Data Bits.

PSTDIV1	PSTDIV0	Description
0	0	$f_{PLL} = f_{VCO}/1$
0	1	$f_{PLL} = f_{VCO}/2$
1	0	$f_{PLL} = f_{VCO}/4$
1	1	$f_{PLL} = f_{VCO}/8$

PLLEN PLL Enable Control Bit

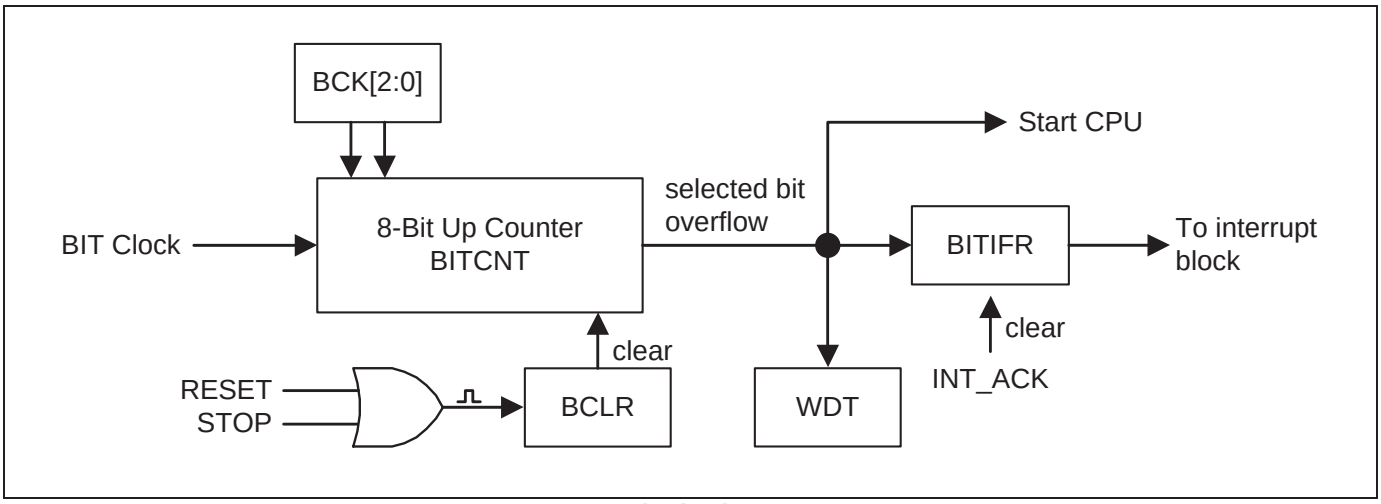
0 PLL Disable

1 PLL Enable

Note: The PLLEN bit won't be cleared to "0b" during the PLL clock is selected as the system clock.

10.2 BASIC INTERVAL TIMER

10.2.1 BLOCK DIAGRAM



BIT Block Diagram

10.2.2 REGISTER MAP

Name	Address	Dir	Default	Description
BITCR	8BH	R/W	01H	Basic Interval Timer Control Register
BITCNT	8CH	R	00H	Basic Interval Timer Counter Register

Register Map

10.2.3 REGISTER DESCRIPTION FOR BASIC INTERVAL TIMER

BITCNT (Basic Interval Timer Counter Register) : 8CH

.7	.6	.5	.4	.3	.2	.1	.0
BITCNT7	BITCNT 6	BITCNT 5	BITCNT 4	BITCNT 3	BITCNT 2	BITCNT 1	BITCNT 0
R	R	R	R	R	R	R	R

Initial value: 00H

BITCNT[7:0] BIT Counter

BITCR (Basic Interval Timer Control Register) : 8BH

.7	.6	.5	.4	.3	.2	.1	.0
BITIFR	BITCK1	BITCK0	–	BCLR	BCK2	BCK1	BCK0
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W

Initial value: 01H

BITIFR When BIT Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 BIT Interrupt no generation

1 BIT Interrupt generation

BITCK[1:0] Select BIT Clock Source

BITCK1	BITCK0	Description
0	0	fx/4096
0	1	fx/1024
1	0	fx/128
1	1	fx/16

BCLR If this bit is written to ‘1’, BIT counter is cleared as ‘0’

0 Free running

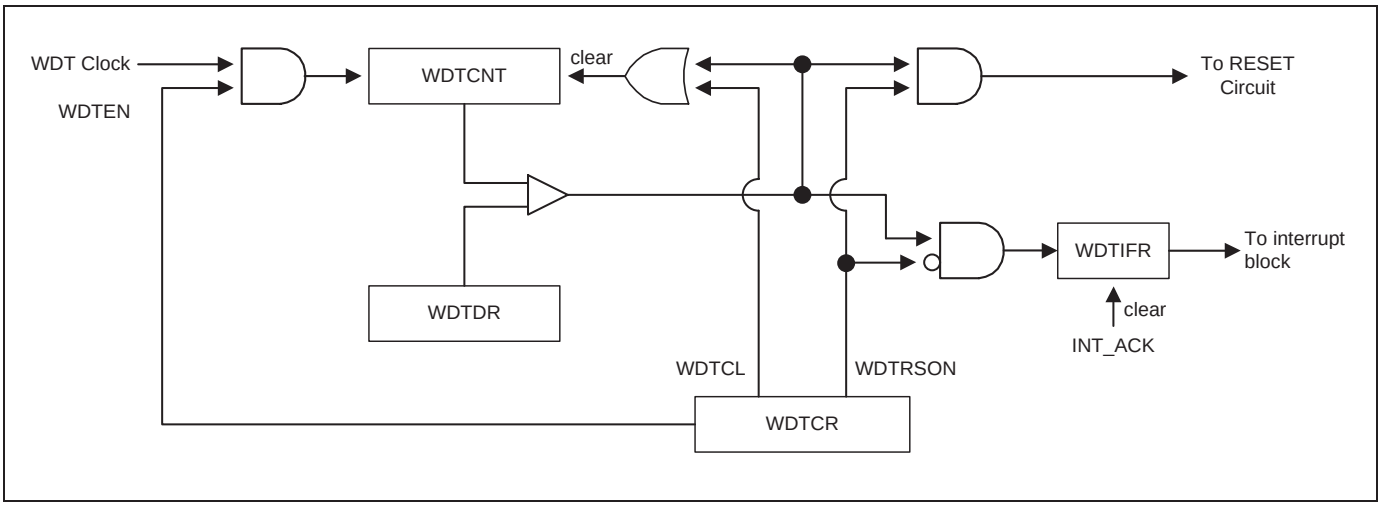
1 Clear counter

BCK[2:0] Select BIT overflow period

BCK2	BCK1	BCK0	description
0	0	0	Bit 0 overflow (BIT Clock *2)
0	0	1	Bit 1 overflow (BIT Clock *4) (default)
0	1	0	Bit 2 overflow (BIT Clock *8)
0	1	1	Bit 3 overflow (BIT Clock *16)
1	0	0	Bit 4 overflow (BIT Clock *32)
1	0	1	Bit 5 overflow (BIT Clock *64)
1	1	0	Bit 6 overflow (BIT Clock *128)
1	1	1	Bit 7 overflow (BIT Clock *256)

10.3 WATCH DOG TIMER

10.3.1 BLOCK DIAGRAM



WDT Block Diagram

10.3.2 REGISTER MAP

Name	Address	Dir	Default	Description
WDTCNT	8EH	R	00H	Watch Dog Timer Counter Register
WDTDR	8EH	W	FFH	Watch Dog Timer Data Register
WDTCR	8DH	R/W	00H	Watch Dog Timer Control Register

Register Map

10.3.3 REGISTER DESCRIPTION FOR WATCH DOG TIMER

WDTCNT (Watch Dog Timer Counter Register : Read Case) : 8EH

.7	.6	.5	.4	.3	.2	.1	.0
WDTCNT7	WDTCNT6	WDTCNT5	WDTCNT4	WDTCNT3	WDTCNT2	WDTCNT1	WDTCNT0
R	R	R	R	R	R	R	R

Initial value: 00H

WDTCNT[7:0] WDT Counter

WDTDR (Watch Dog Timer Data Register : Write Case) : 8EH

.7	.6	.5	.4	.3	.2	.1	.0
WDTDR7	WDTDR6	WDTDR5	WDTDR4	WDTDR3	WDTDR2	WDTDR1	WDTDR0
W	W	W	W	W	W	W	W

Initial value: FFH

WDTDR[7:0] Set a period

WDT Interrupt Interval=(BIT Interrupt Interval)X(WDTDR Value +1)

Note: Do not write “0” in the WDTDR register

WDTCR (Watch Dog Timer Control Register) : 8DH

.7	.6	.5	.4	.3	.2	.1	.0
WDTEN	WDTRSON	WDTCL	–	–	–	WDTCK	WDTIFR
R/W	R/W	R/W	–	–	–	R/W	R/W

Initial value: 00H

WDTEN Control WDT operation

0 Disable

1 Enable

WDTRSON Control WDT RESET operation

0 Free running 8-bit timer

1 Watch Dog Timer RESET ON

WDTCL Clear WDT Counter

0 Free run

1 Clear WDT Counter (auto clear after 1 cycle)

WDTCK Control WDT Clock Selection Bit

0 BIT overflow for WDT clock (WDTRC disable)

1 WDTRC for WDT clock (WDTRC enable)

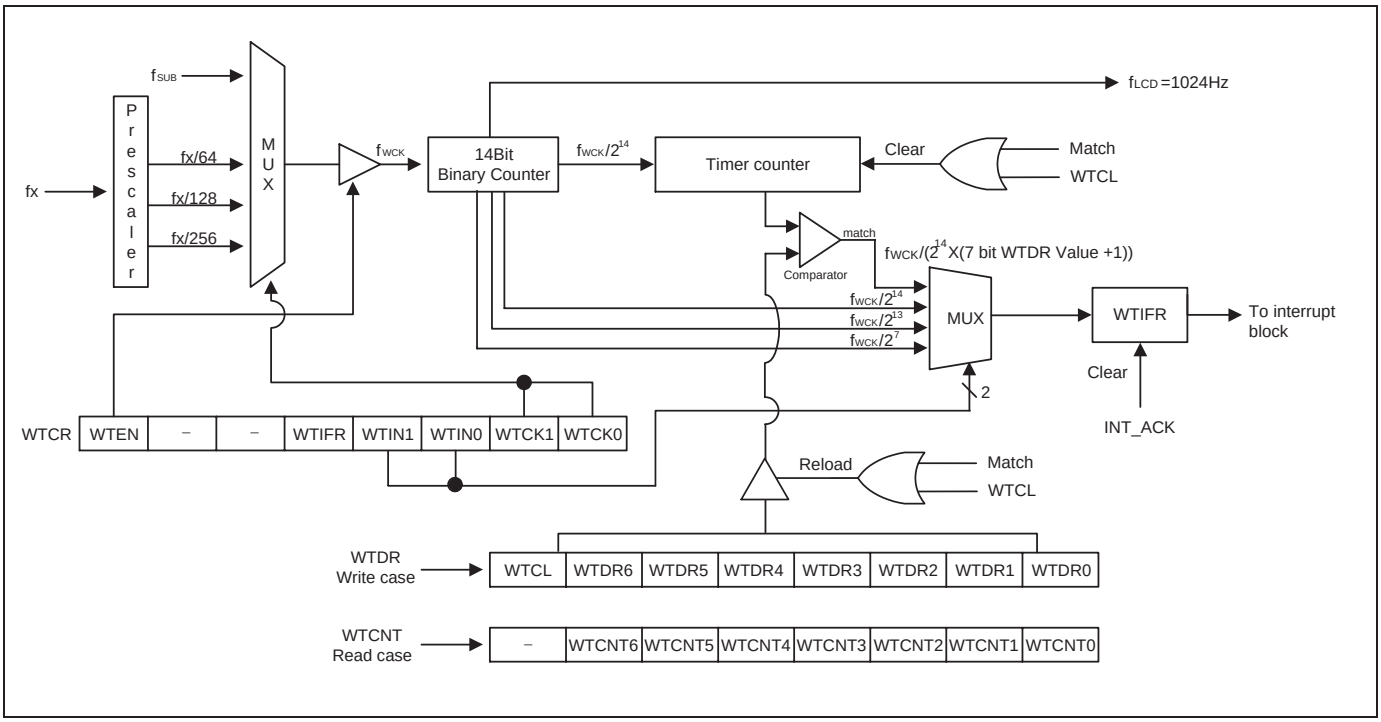
WDTIFR When WDT Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 WDT Interrupt no generation

1 WDT Interrupt generation

10.4 WATCH TIMER

10.4.1 BLOCK DIAGRAM



Watch Timer Block Diagram

10.4.2 REGISTER MAP

Name	Address	Dir	Default	Description
WTCNT	9FH	R	00H	Watch Timer Counter Register
WTDR	9FH	W	7FH	Watch Timer Data Register
WTCR	9EH	R/W	00H	Watch Timer Control Register

Register Map

10.4.3 REGISTER DESCRIPTION FOR WATCH TIMER

WTCNT (Watch Timer Counter Register : Read Case) : 9FH

.7	.6	.5	.4	.3	.2	.1	.0
–	WTCNT6	WTCNT5	WTCNT4	WTCNT3	WTCNT2	WTCNT1	WTCNT0
–	R	R	R	R	R	R	R

Initial value: 00H

WTCNT[6:0] WT Counter

WTDR (Watch Timer Data Register : Write Case) : 9FH

.7	.6	.5	.4	.3	.2	.1	.0
WTCL	WTDR6	WTDR5	WTDR4	WTDR3	WTDR2	WTDR1	WTDR0
R/W	W	W	W	W	W	W	W

Initial value: 7FH

WTCL Clear WT Counter

0 Free Run

1 Clear WT Counter (auto clear after 1 cycle)

WTDR[6:0] Set WT period

WT Interrupt interval = fwck/(2^14 X (7bit WTDR Value +1))

Note: Do not write “0” in the WTDR register.

WTCR (Watch Timer Control Register) : 9EH

.7	.6	.5	.4	.3	.2	.1	.0
WTEN	–	–	WTIFR	WTIN1	WTIN0	WTCK1	WTCK0
R/W	–	–	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

WTEN Control Watch Timer

0 Disable

1 Enable

WTIFR When WT Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 WT Interrupt no generation

1 WT Interrupt generation

WTIN[1:0] Determine interrupt interval

WTIN1	WTIN0	description
0	0	fwck/2^7
0	1	fwck/2^13
1	0	fwck/2^14
1	1	fwck/(2^14 X (7bit WTDR Value + 1))

WTCK[1:0] Determine source clock

WTCK1	WTCK0	description
0	0	f_{SUB}
0	1	fx/256
1	0	fx/128
1	1	fx/64

Note: fx – System clock frequency (where fx=4.19MHz)

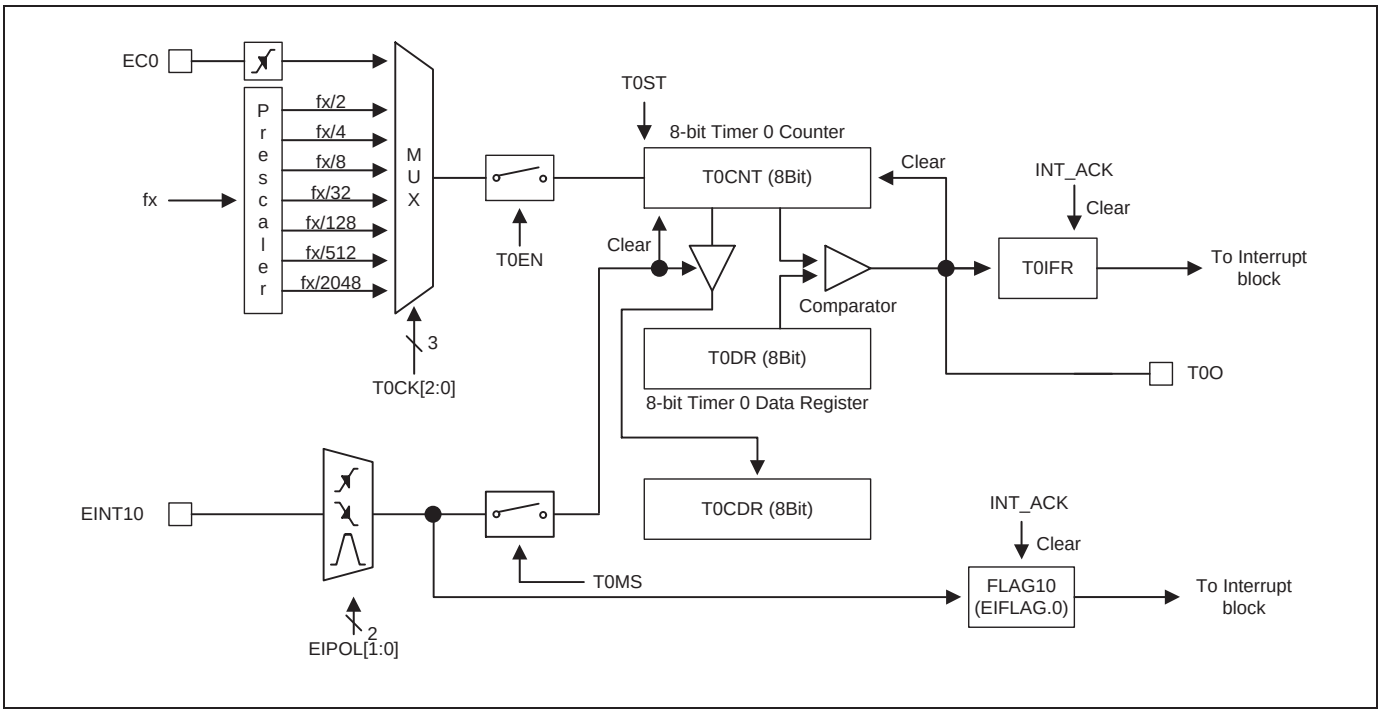
fsub – Sub clock oscillator frequency (32.768KHz)

fwck – Selected Watch Timer clock

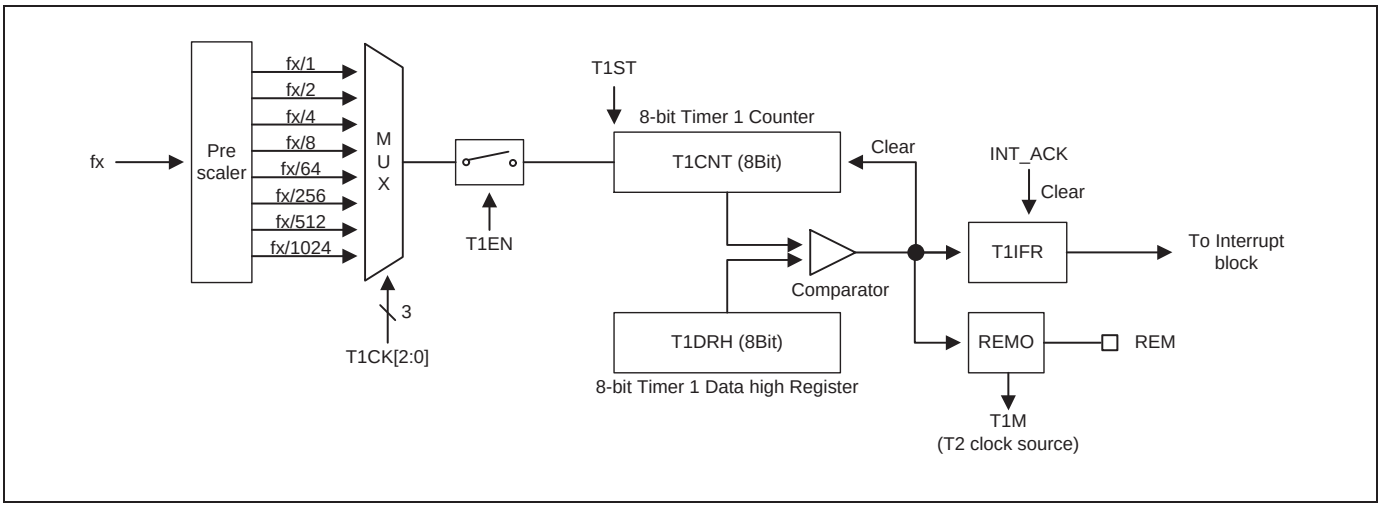
fLCD – LCD frequency (where fx=4.19MHz, WTCK[1:0]=’10’; fLCD = 1024Hz)

10.5 TIMER 0, 1

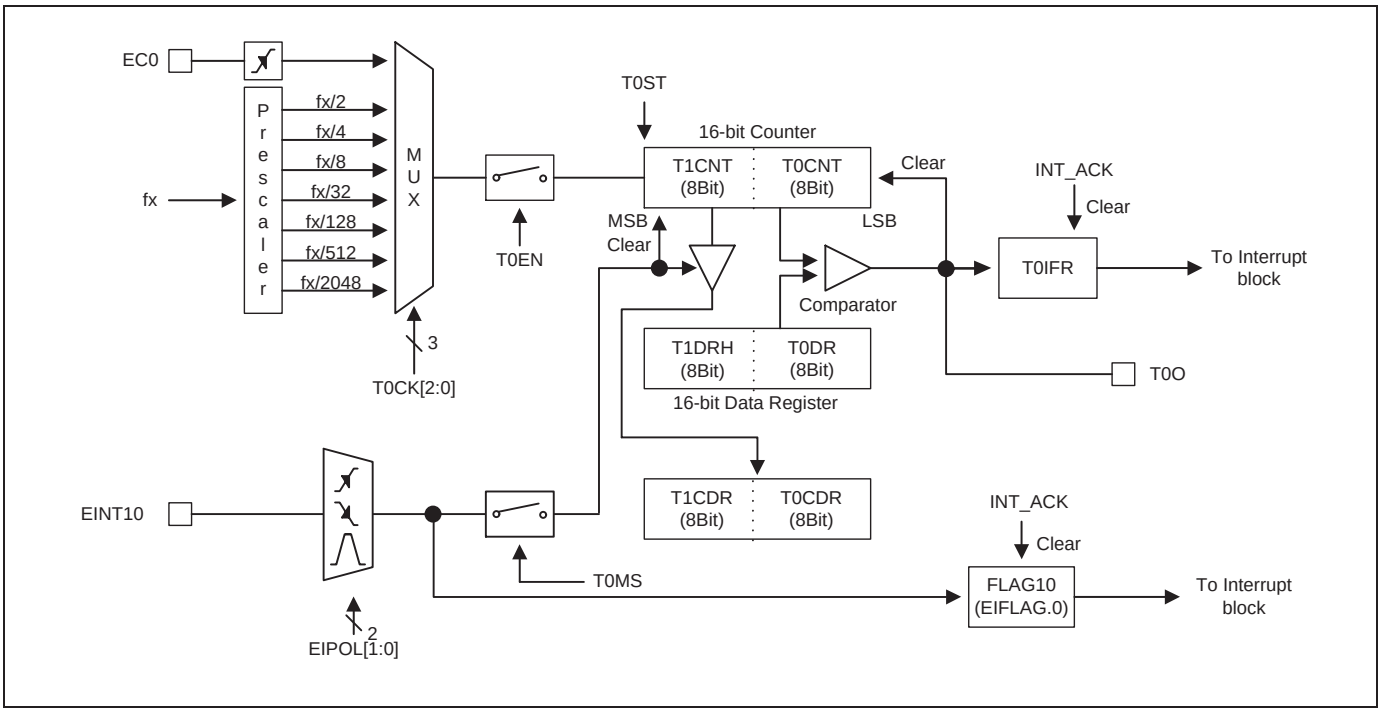
10.5.1 BLOCK DIAGRAM



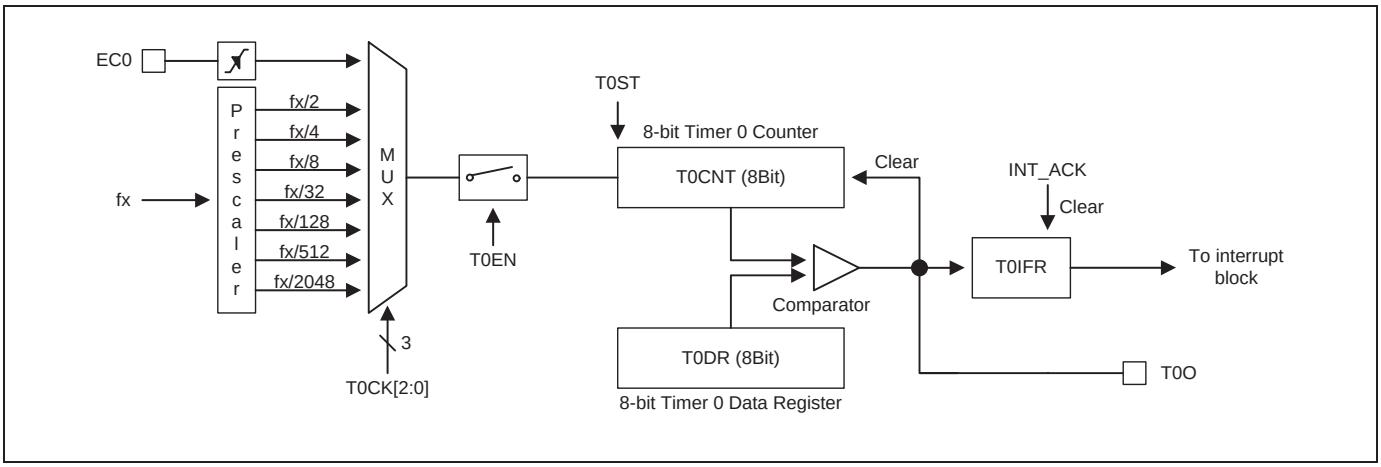
8-Bit Timer/Event Counter 0 Block Diagram



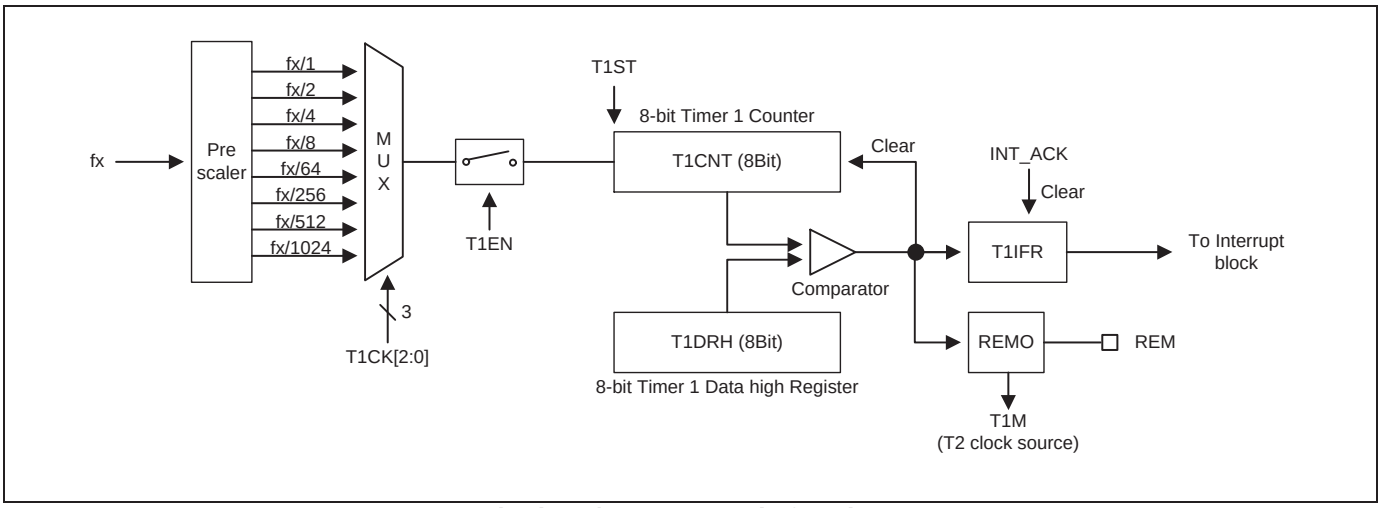
8-Bit Timer Counter 1 Block Diagram



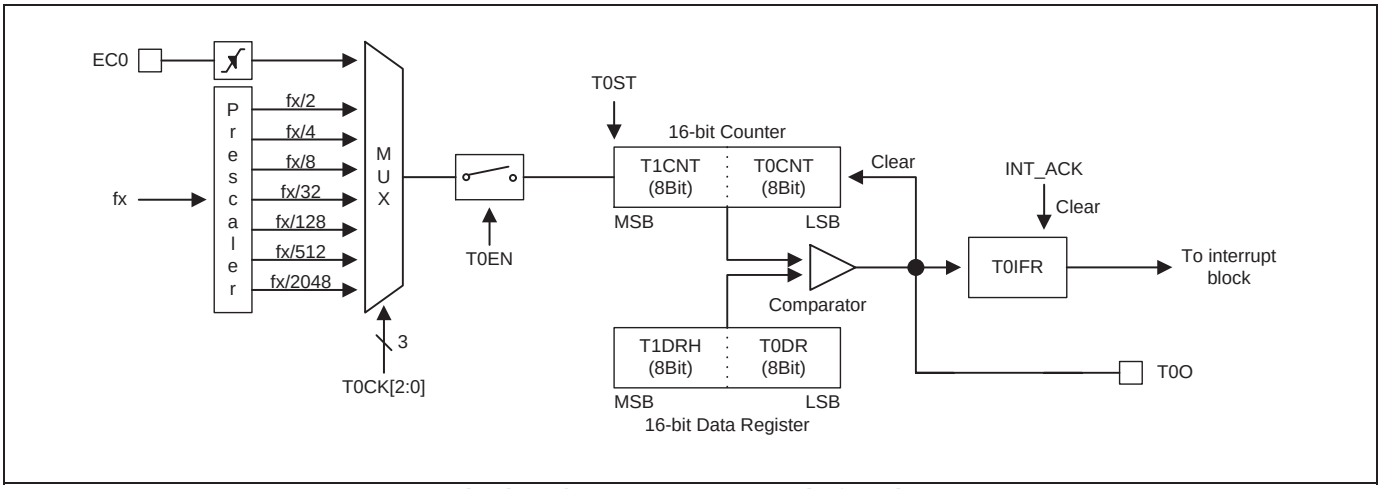
16-Bit Timer/Event Counter 0 Block Diagram



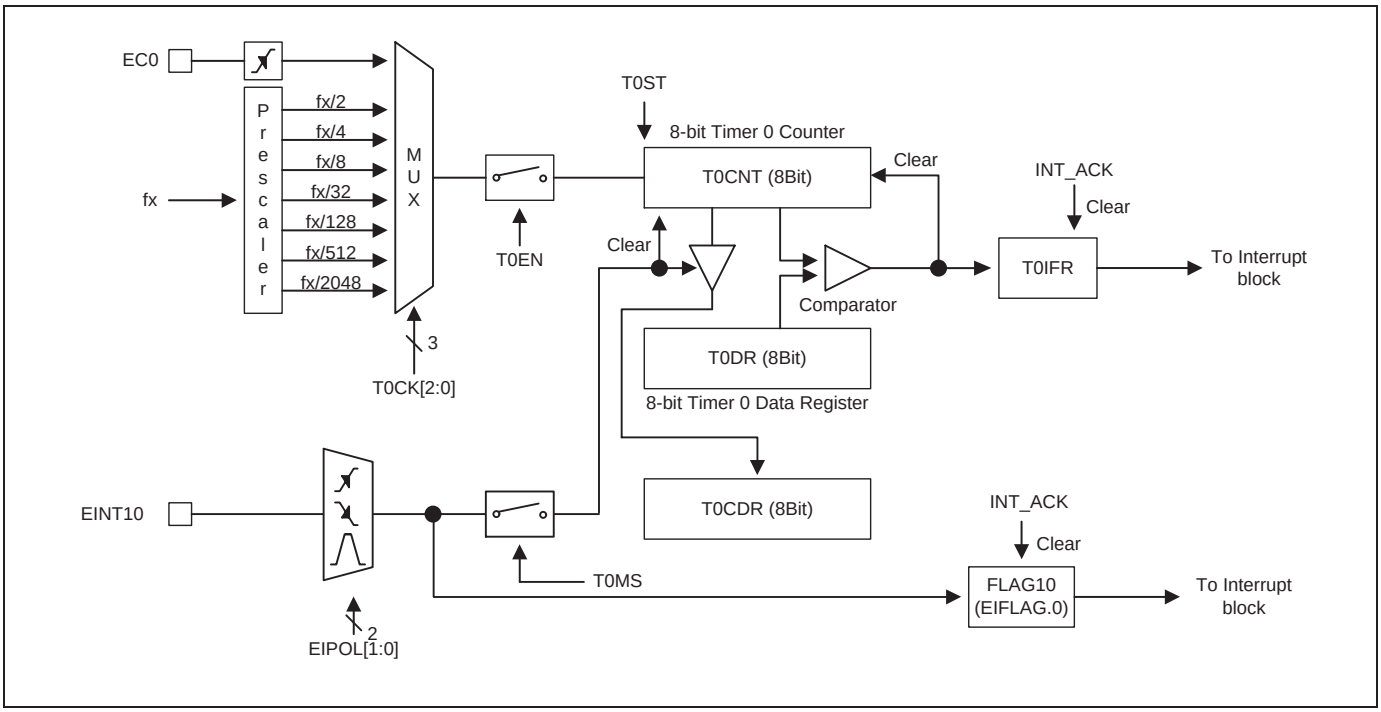
8-Bit Timer/Event Mode for Timer 0



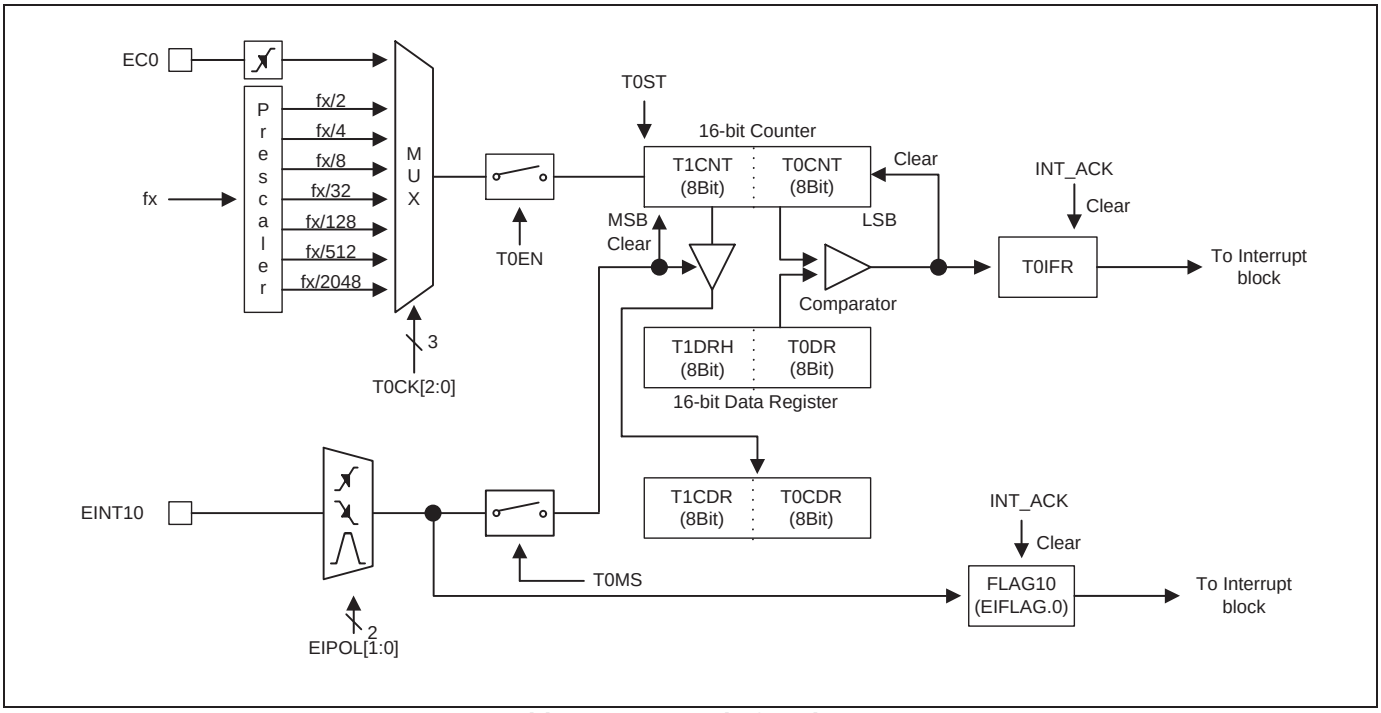
8-Bit Timer/Counter Mode for Timer 1



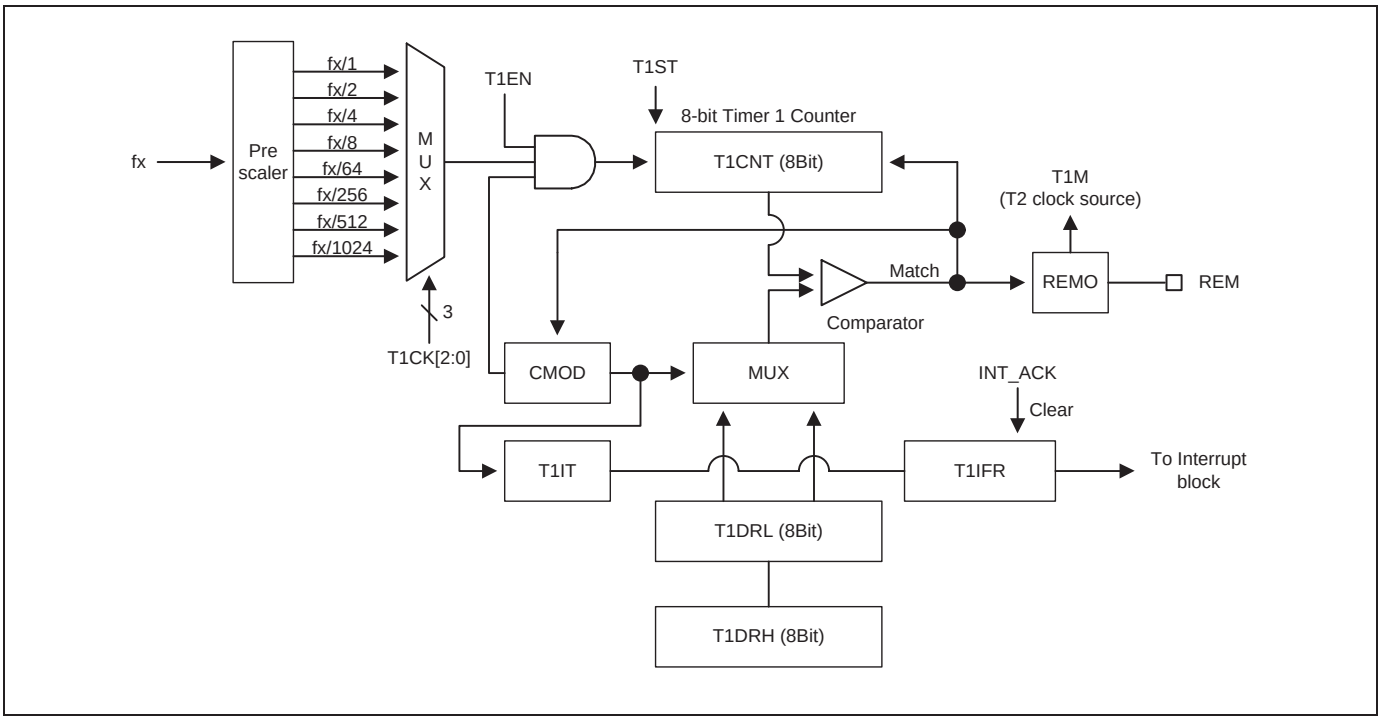
16-Bit Timer/Event Counter Mode for Timer 0



8-bit Capture Mode for Timer 0



16-bit Capture Mode for Timer 0



Carrier Mode for Timer 1

10.5.2 REGISTER MAP

Name	Address	Dir	Default	Description
T0CNT	B3H	R	00H	Timer 0 Counter Register
T0DR	B4H	R/W	FFH	Timer 0 Data Register
T0CDR	B4H	R	00H	Timer 0 Capture Data Register
T0CR	B2H	R/W	00H	Timer 0 Control Register
T1CNT	CBH	R	00H	Timer 1 Counter Register
T1DRH	CDH	R/W	FFH	Timer 1 Data High Register
T1DRL	CCH	R/W	FFH	Timer 1 Data Low Register
T1CDR	CDH	R	00H	Timer 1 Capture Data Register
T1CR	CAH	R/W	00H	Timer 1 Control Register
CARCR	CEH	R/W	00H	Carrier Mode control Register

Register Map

10.5.3 REGISTER DESCRIPTION FOR TIMER 0, 1

T0CNT (Timer 0 Counter Register) : B3H

.7	.6	.5	.4	.3	.2	.1	.0
T0CNT7	T0CNT6	T0CNT5	T0CNT4	T0CNT3	T0CNT2	T0CNT1	T0CNT0
R	R	R	R	R	R	R	R

Initial value: 00H

T0CNT[7:0] T0 Counter

T0DR (Timer 0 Data Register : Write Case) : B4H

.7	.6	.5	.4	.3	.2	.1	.0
T0DR7	T0DR6	T0DR5	T0DR4	T0DR3	T0DR2	T0DR1	T0DR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T0DR[7:0] T0 Data

T0CDR (Timer 0 Capture Data Register : Read Case, Capture mode only) : B4H

.7	.6	.5	.4	.3	.2	.1	.0
T0CDR7	T0CDR6	T0CDR5	T0CDR4	T0CDR3	T0CDR2	T0CDR1	T0CDR0
R	R	R	R	R	R	R	R

Initial value: 00H

T0CDR[7:0] T0 Capture

T0CR (Timer 0 Control Register) : B2H

.7	.6	.5	.4	.3	.2	.1	.0
T0EN	–	T0MS	T0CK2	T0CK1	T0CK0	T0CN	T0ST
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

T0EN Control Timer 0

0 Timer 0 disable

1 Timer 0 enable

T0MS Control Timer 0 Operation Mode

0 Timer/counter mode

1 Capture mode

T0CK[2:0] Select Timer 0 clock source. fx is main system clock frequency

T0CK2	T0CK1	T0CK0	description
0	0	0	fx/2
0	0	1	fx/4
0	1	0	fx/8
0	1	1	fx/32
1	0	0	fx/128
1	0	1	fx/512
1	1	0	fx/2048
1	1	1	External Clock (EC0)

T0CN Control Timer 0 Counter pause/continue

0 Temporary count stop

1 Continue count

T0ST Control Timer 0 start/stop

0 Counter stop

1 Clear counter and start

T1CNT (Timer 1 Counter Register) : CBH

.7	.6	.5	.4	.3	.2	.1	.0
T1CNT7	T1CNT6	T1CNT5	T1CNT4	T1CNT3	T1CNT2	T1CNT1	T1CNT0
R	R	R	R	R	R	R	R

Initial value: 00H

T1CNT[7:0] T1 Counter

T1DRH (Timer 1 Data High Register) : CDH

.7	.6	.5	.4	.3	.2	.1	.0
T1DRH7	T1DRH6	T1DRH5	T1DRH4	T1DRH3	T1DRH2	T1DRH1	T1DRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T1DRH[7:0] T1 High Data

T1DRL (Timer 1 Data Low Register : Carrier mode only) : CCH

.7	.6	.5	.4	.3	.2	.1	.0
T1DRL7	T1DRL6	T1DRL5	T1DRL4	T1DRL3	T1DRL2	T1DRL1	T1DRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T1DRL[7:0] T1 Low Data

T1CDR (Timer 1 Capture Data Register : Read Case, 16bit Capture mode only) : CDH

.7	.6	.5	.4	.3	.2	.1	.0
T1CDR7	T1CDR6	T1CDR5	T1CDR4	T1CDR3	T1CDR2	T1CDR1	T1CDR0
R	R	R	R	R	R	R	R

Initial value: 00H

T1CDR[7:0] 16bit T0 Capture

T1CR (Timer 1 Control Register) : CAH

.7	.6	.5	.4	.3	.2	.1	.0
T1EN	16BIT0	T1MS	T1CK2	T1CK1	T1CK0	T1CN	T1ST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

T1EN Control Timer 1

0 Timer 1 disable

1 Timer 1 enable

16BIT0 Select Timer 0 8/16Bit

0 8 bit

1 16 bit

T1MS Control Timer 1 operation mode

0 Timer/counter mode

1 Carrier mode

T1CK[2:0] Select Timer 1 clock source. fx is main system clock frequency

T1CK2	T1CK1	T1CK0	description
0	0	0	fx/1
0	0	1	fx/2
0	1	0	fx/4
0	1	1	fx/8
1	0	0	fx/64
1	0	1	fx/256
1	1	0	fx/512
1	1	1	fx/1024

T1CN Control Timer 1 Counter pause/continue

0 Temporary count stop

1 Continue count

T1ST Control Timer 1 start/stop

0 Counter stop

1 Clear counter and start

CARCR (Carrier Mode Control Register : Carrier mode only) : CEH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	T1IT1	T1IT0	–	–	CMOD	REMO
–	–	R/W	R/W	–	–	R/W	R/W

Initial value: 00H

T1IT[1:0] T1 Interrupt time select

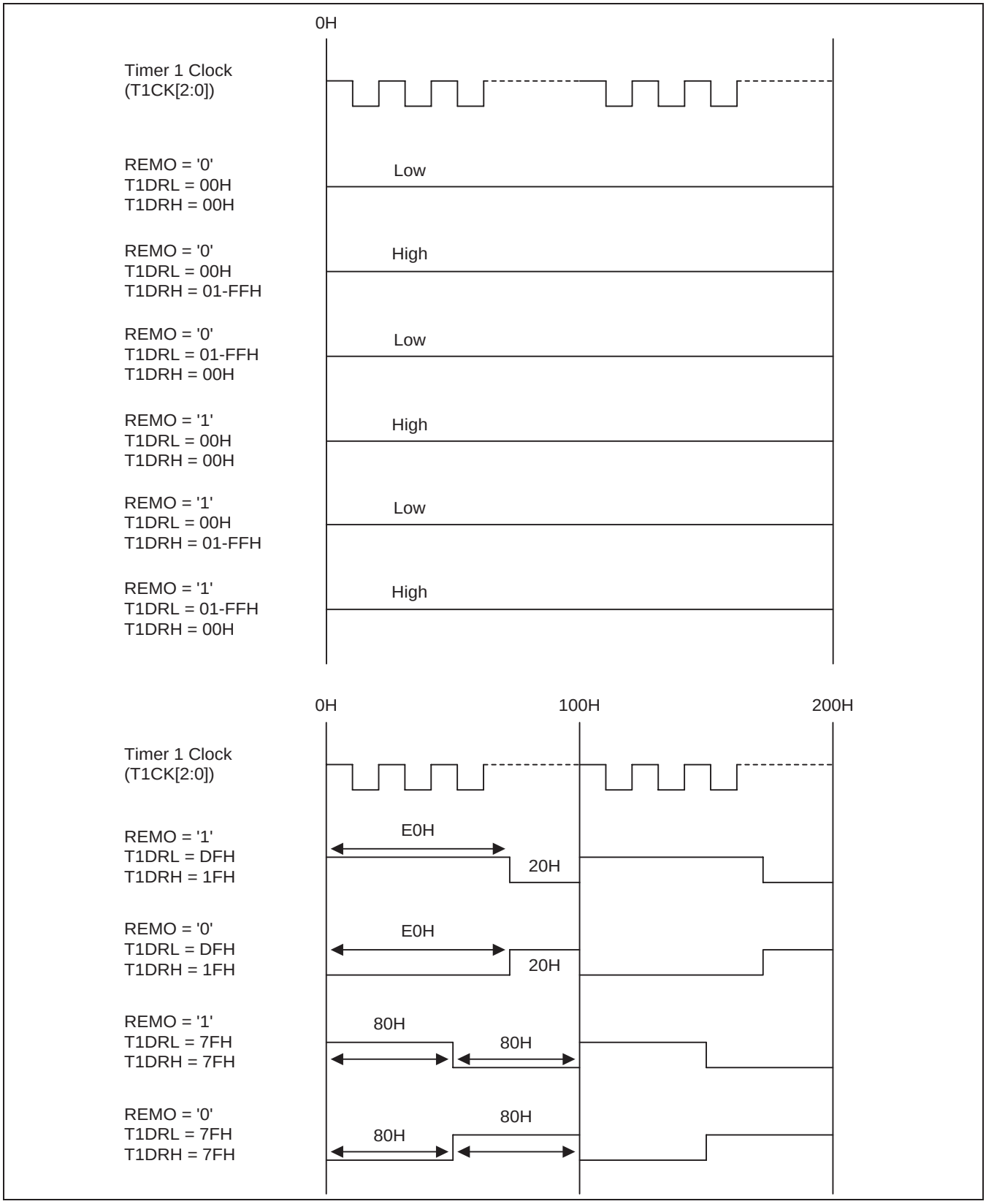
T1IT1	T1IT0	description
0	0	Elapsed time for low data value
0	1	Elapsed time for high data value
1	0	Elapsed time for low and high data values
1	1	Not available

CMOD Carrier Frequency Mode Select

0	One-shot mode
1	Repeating mode

REMO REM Output Control

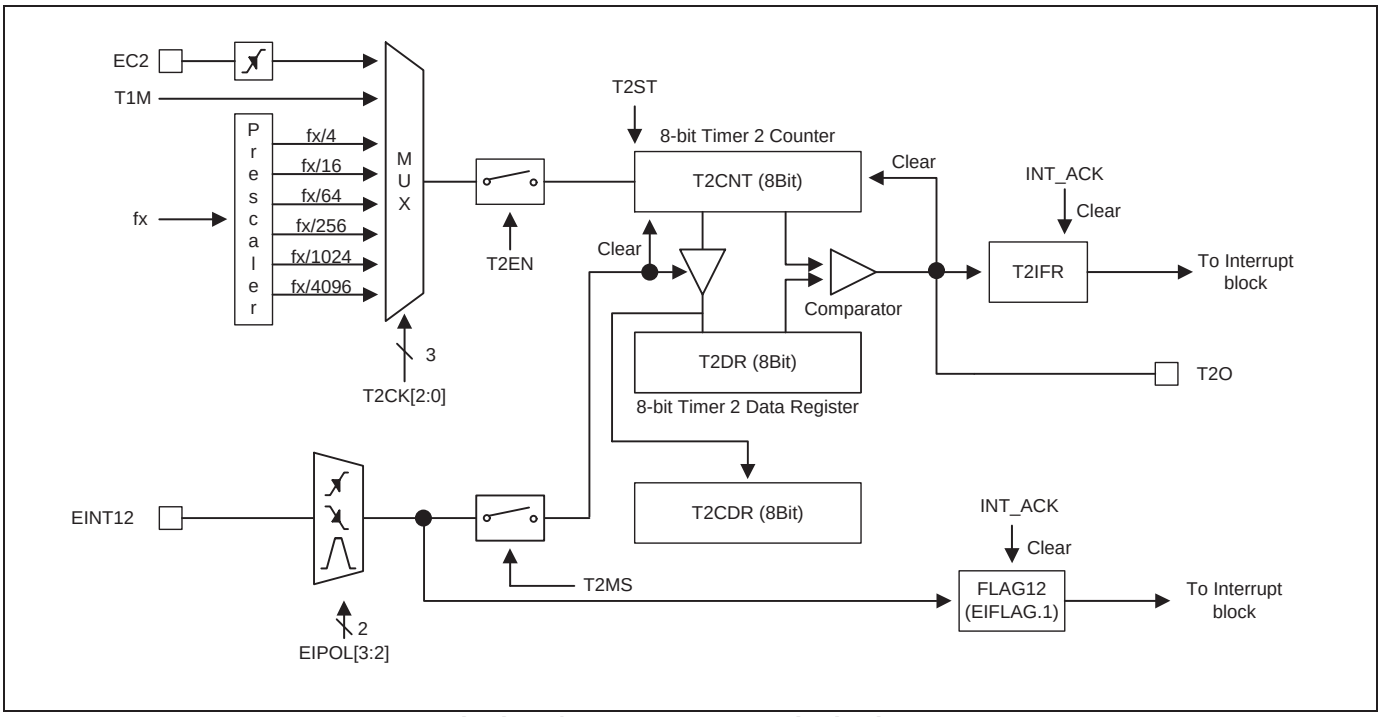
0	T1DRL -> Low width, T1DRH -> High width
1	T1DRL -> High width, T1DRH -> Low width



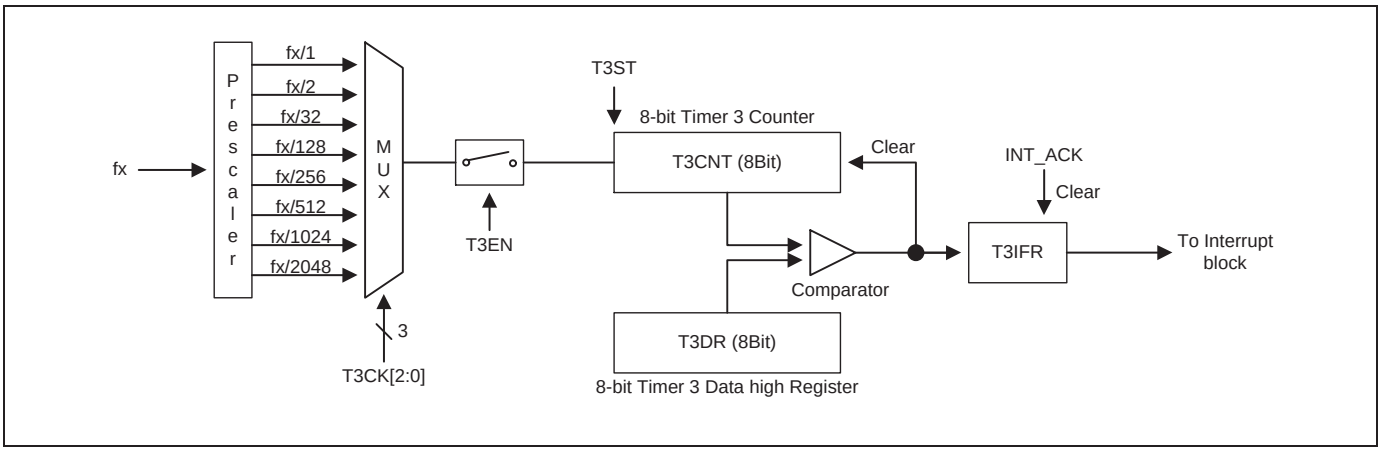
Carrier Output Waveforms in Repeat Mode for Timer 1

10.6 TIMER 2, 3

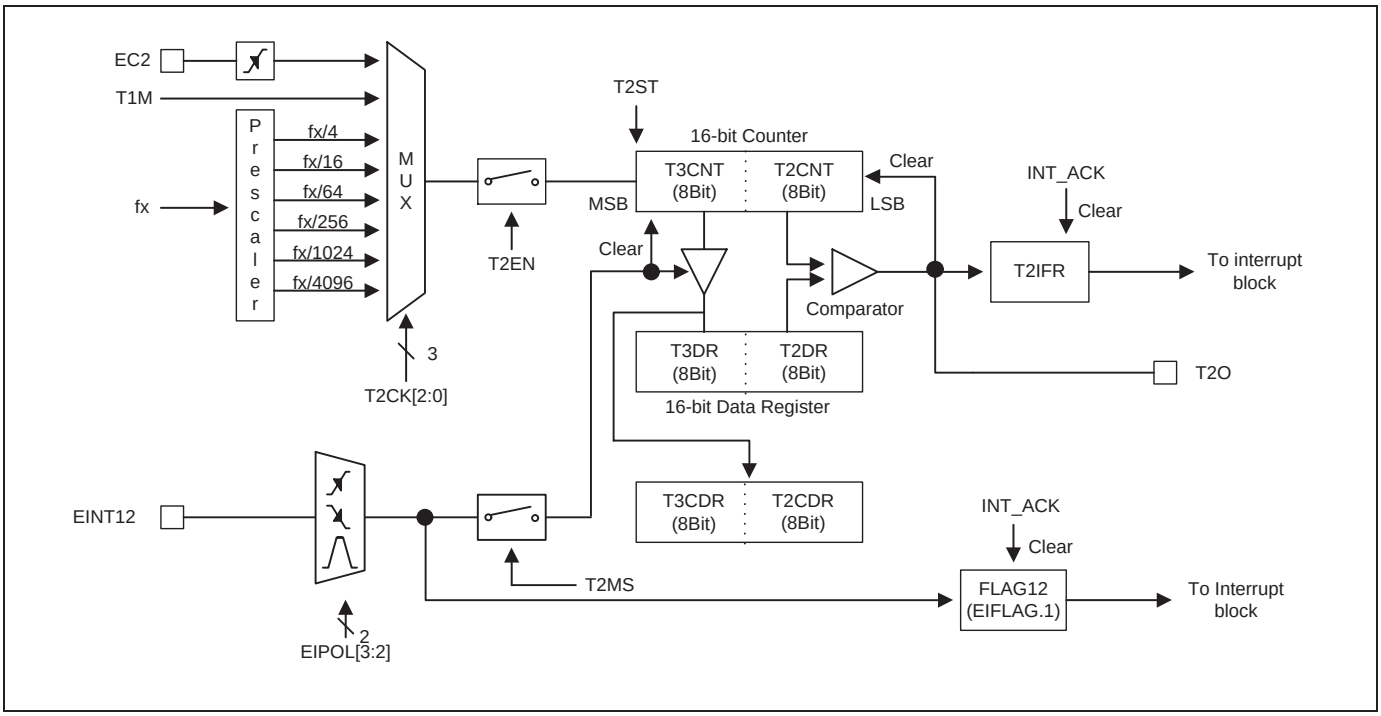
10.6.1 BLOCK DIAGRAM



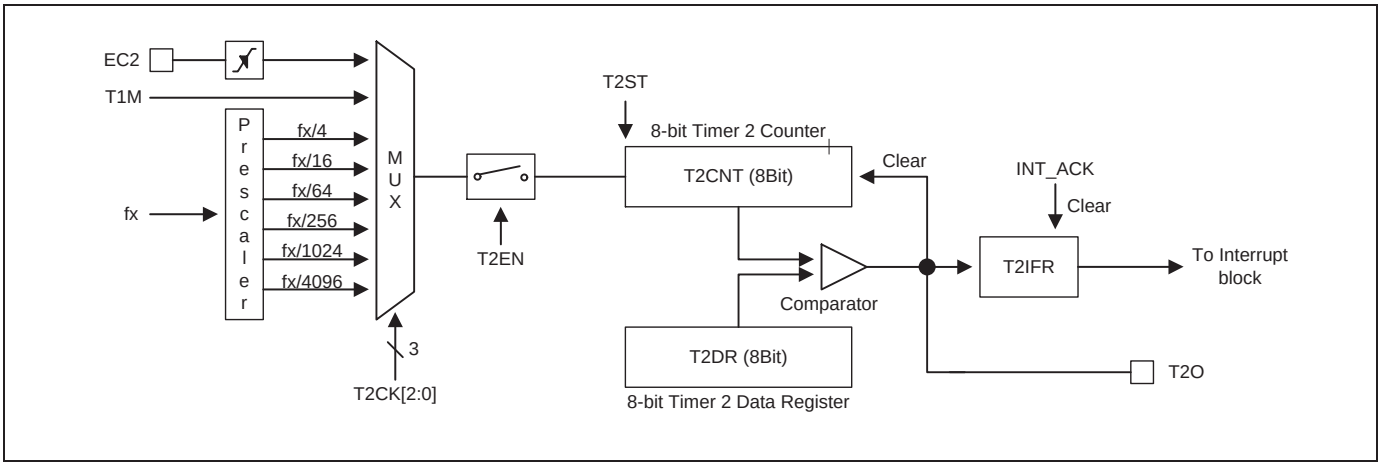
8-Bit Timer/Event Counter 2 Block Diagram



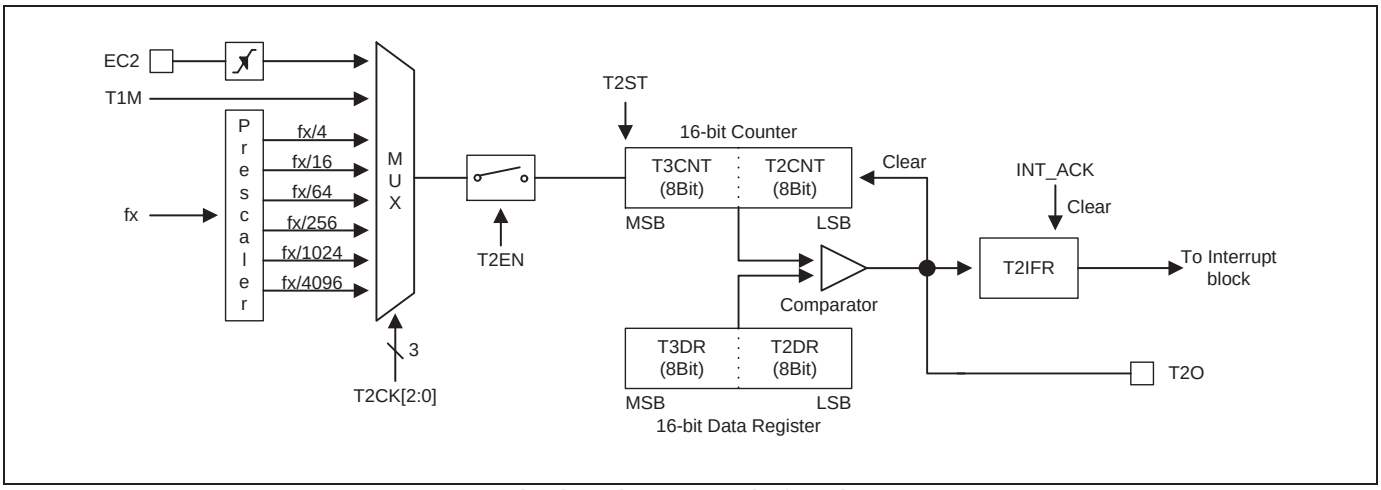
8-Bit Timer Counter 3 Block Diagram



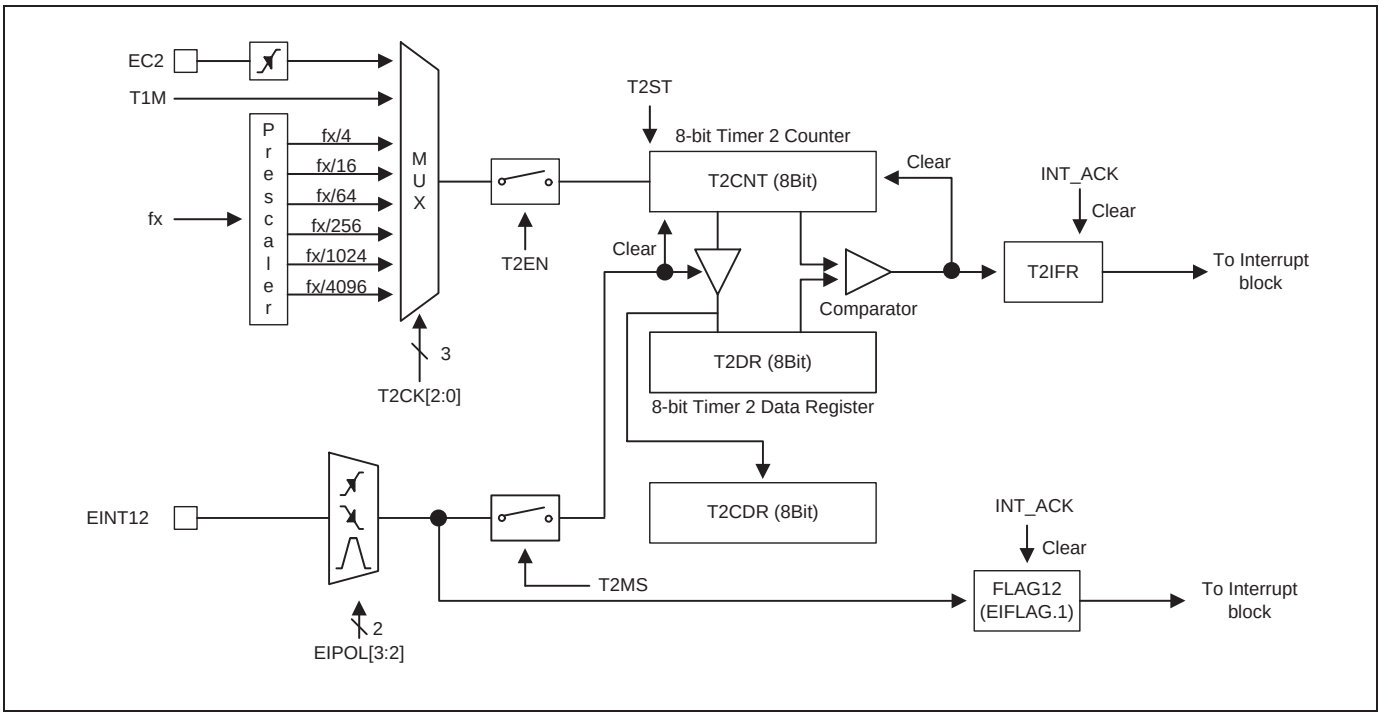
16-Bit Timer/Event Counter 2 Block Diagram



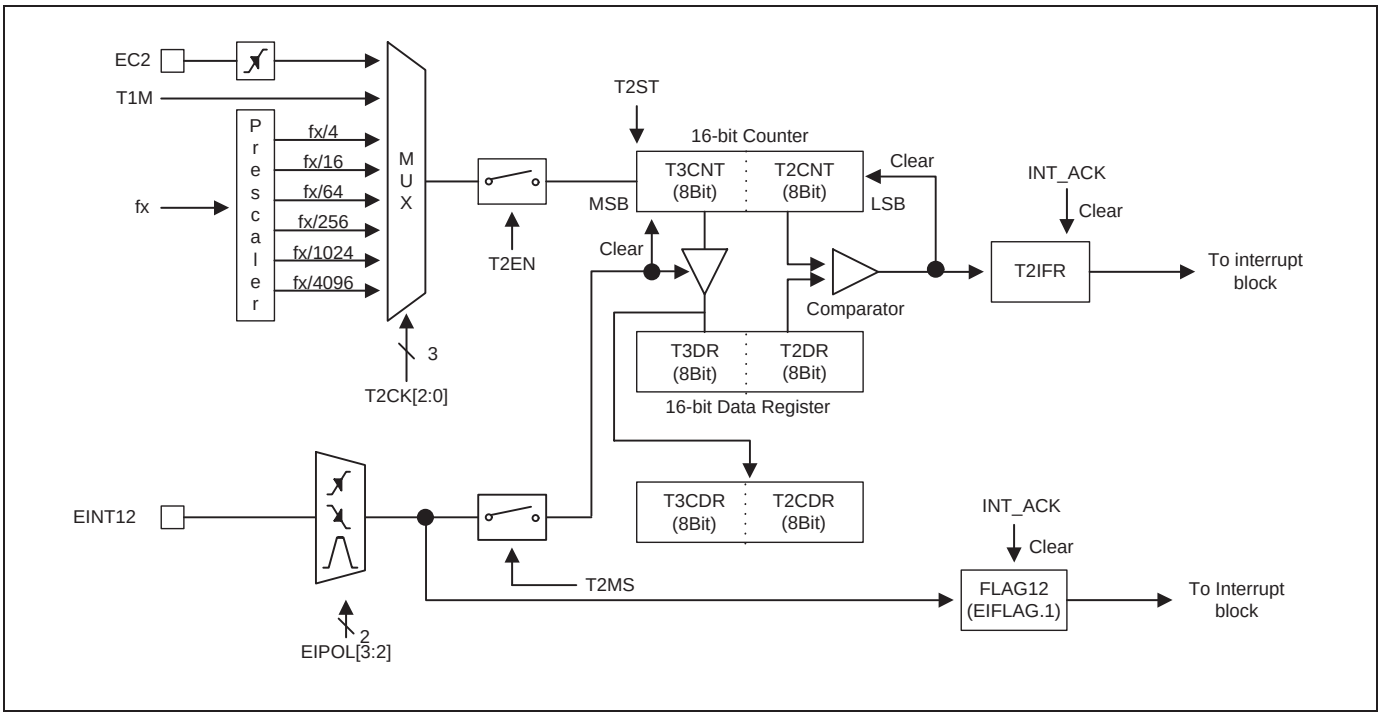
8-Bit Timer/Event Mode for Timer 2



16-Bit Timer/Event Mode for Timer 2



8-bit Capture Mode for Timer 2



16-bit Capture Mode for Timer 2

10.6.2 REGISTER MAP

Name	Address	Dir	Default	Description
T2CNT	BCH	R	00H	Timer 2 Counter Register
T2DR	BEH	R/W	FFH	Timer 2 Data Register
T2CDR	BEH	R	00H	Timer 2 Capture Data Register
T2CR	BAH	R/W	00H	Timer 2 Control Register
T3CNT	C4H	R	00H	Timer 3 Counter Register
T3DR	C6H	R/W	FFH	Timer 3 Data Register
T3CDR	C6H	R	00H	Timer 3 Capture Data Register
T3CR	C2H	R/W	00H	Timer 3 Control Register
TIFR	C3H	R/W	00H	Timer Interrupt Flag Register

Register Map

10.6.3 REGISTER DESCRIPTION FOR TIMER 2, 3

T2CNT (Timer 2 Counter Register) : BCH

.7	.6	.5	.4	.3	.2	.1	.0
T2CNT7	T2CNT6	T2CNT5	T2CNT4	T2CNT3	T2CNT2	T2CNT1	T2CNT0
R	R	R	R	R	R	R	R

Initial value: 00H

T2CNT[7:0] T2 Counter

T2DR (Timer 2 Data Register) : BEH

.7	.6	.5	.4	.3	.2	.1	.0
T2DR7	T2DR6	T2DR5	T2DR4	T2DR3	T2DR2	T2DR1	T2DR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T2DR[7:0] T2 Data

T2CDR (Timer 2 Capture Data Register : Read Case, Capture mode only) : BEH

.7	.6	.5	.4	.3	.2	.1	.0
T2CDR7	T2CDR6	T2CDR5	T2CDR4	T2CDR3	T2CDR2	T2CDR1	T2CDR0
R	R	R	R	R	R	R	R

Initial value: 00H

T2CDR[7:0] T2 Capture

T2CR (Timer 2 Control Register) : BAH

.7	.6	.5	.4	.3	.2	.1	.0
T2EN	–	T2MS	T2CK2	T2CK1	T2CK0	T2CN	T2ST
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

T2EN Control Timer 2

0 Timer 2 disable

1 Timer 2 enable

T2MS Control Timer 2 Operation Mode

0 Timer/counter mode

1 Capture mode

T2CK[2:0] Select Timer 2 clock source. fx is main system clock frequency

T2CK2	T2CK1	T2CK0	description
0	0	0	T1M
0	0	1	fx/4
0	1	0	fx/16
0	1	1	fx/64
1	0	0	fx/256
1	0	1	fx/1024
1	1	0	fx/4096
1	1	1	External Clock (EC2)

T2CN Control Timer 2 Counter pause/continue

0 Temporary count stop

1 Continue count

T2ST Control Timer 2 start/stop

0 Counter stop

1 clear counter and start

T3CNT (Timer 3 Counter Register) : C4H

.7	.6	.5	.4	.3	.2	.1	.0
T3CNT7	T3CNT6	T3CNT5	T3CNT4	T3CNT3	T3CNT2	T3CNT1	T3CNT0
R	R	R	R	R	R	R	R

Initial value: 00H

T3CNT[7:0] T3 Counter

T3DR (Timer 3 Data Register) : C6H

.7	.6	.5	.4	.3	.2	.1	.0
T3DR7	T3DR6	T3DR5	T3DR4	T3DR3	T3DR2	T3DR1	T3DR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T3DR[7:0] T3 Data

T3CDR (Timer 3 Capture Data Register : Read Case, 16bit Capture mode only) : C6H

.7	.6	.5	.4	.3	.2	.1	.0
T3CDR7	T3CDR6	T3CDR5	T3CDR4	T3CDR3	T3CDR2	T3CDR1	T3CDR0
R	R	R	R	R	R	R	R

Initial value: 00H

T3CDR[7:0] 16bit T2 Capture

T3CR (Timer 3 Mode Control Register) : C2H

.7	.6	.5	.4	.3	.2	.1	.0
T3EN	16BIT2	–	T3CK2	T3CK1	T3CK0	T3CN	T3ST
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

T3EN Control Timer 3

0 Timer 3 disable

1 Timer 3 enable

16BIT2 Select Timer 2 8/16Bit

0 8 bit

1 16 bit

T3CK[2:0] Select Timer 3 clock source. fx is main system clock frequency

T3CK2	T3CK1	T3CK0	description
0	0	0	fx/1
0	0	1	fx/2
0	1	0	fx/32
0	1	1	fx/128
1	0	0	fx/256
1	0	1	fx/512
1	1	0	fx/1024
1	1	1	fx/2048

T3CN Control Timer 3 Counter pause/continue

0 Temporary count stop

1 Continue count

T3ST Control Timer 3 start/stop

0 Counter stop

1 Clear counter and start

TIFR (Timer Interrupt Flag Register) : C3H

.7	.6	.5	.4	.3	.2	.1	.0
SIOIFR	–	–	–	T3IFR	T2IFR	T1IFR	T0IFR
R/W	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

SIOIFR When SIO Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 SIO Interrupt no generation

1 SIO Interrupt generation

T3IFR When T3 Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 T3 Interrupt no generation

1 T3 Interrupt generation

T2IFR When T2 Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 T2 Interrupt no generation

1 T2 Interrupt generation

T1IFR When T1 Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 T1 Interrupt no generation

1 T1 Interrupt generation

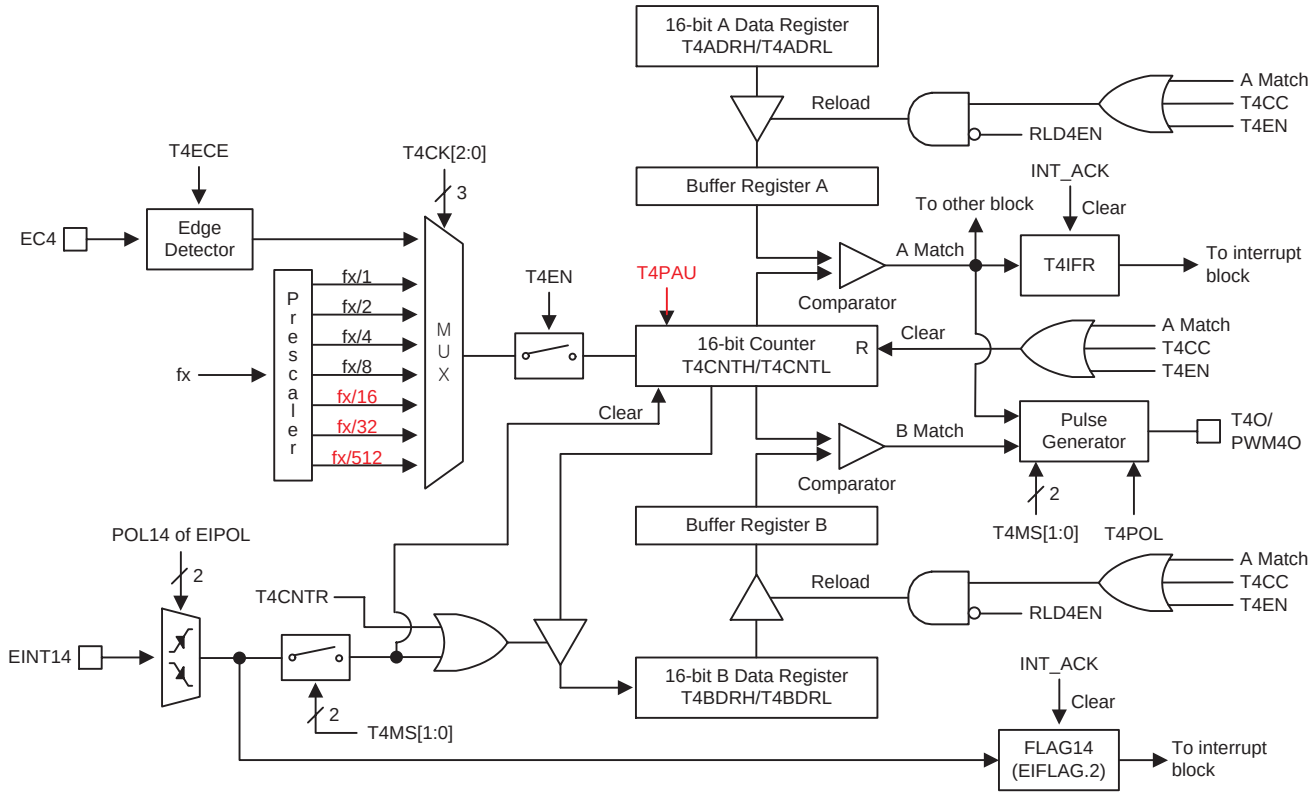
T0IFR When T0 Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal. Writing “1” has no effect.

0 T0 Interrupt no generation

1 T0 Interrupt generation

10.7 16-BIT TIMER COUNTER 4

10.7.1 BLOCK DIAGRAM



Note: The T4EN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.

16-Bit Timer Counter 4 Block Diagram

10.7.2 REGISTER MAP

Name	Address	Dir	Default	Description
T4CRH	C9H	R/W	00H	Timer 4 Control High Register
T4CRL	C8H	R/W	00H	Timer 4 Control Low Register
T4ADRH	D3H	R/W	FFH	Timer 4 A Data High Register
T4ADRL	D2H	R/W	FFH	Timer 4 A Data Low Register
T4BDRH	DFH	R/W	FFH	Timer 4 B Data High Register
T4BDRL	DEH	R/W	FFH	Timer 4 B Data Low Register

Register Map

10.7.3 REGISTER DESCRIPTION FOR TIMER 4

T4ADRH (Timer 4 A Data High Register) : D3H

.7	.6	.5	.4	.3	.2	.1	.0
T4ADRH7	T4ADRH6	T4ADRH5	T4ADRH4	T4ADRH3	T4ADRH2	T4ADRH1	T4ADRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T4ADRH[7:0] T4 A Data High Byte

T4ADRL (Timer 4 A Data Low Register) : D2H

.7	.6	.5	.4	.3	.2	.1	.0
T4ADRL7	T4ADRL6	T4ADRL5	T4ADRL4	T4ADRL3	T4ADRL2	T4ADRL1	T4ADRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T4ADRL[7:0] T4 A Data Low Byte

Note) Do not write “0000H” in the T4ADRH/T4ADRL register when PPG mode.

T4BDRH (Timer 4 B Data High Register) : DFH

.7	.6	.5	.4	.3	.2	.1	.0
T4BDRH7	T4BDRH6	T4BDRH5	T4BDRH4	T4BDRH3	T4BDRH2	T4BDRH1	T4BDRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T4BDRH[7:0] T4 B Data High Byte

T4BDRL (Timer 4 B Data Low Register) : DEH

.7	.6	.5	.4	.3	.2	.1	.0
T4BDRL7	T4BDRL6	T4BDRL5	T4BDRL4	T4BDRL3	T4BDRL2	T4BDRL1	T4BDRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

T4BDRL[7:0] T4 B Data Low Byte

T4CRH (Timer 4 Control High Register) : C9H

.7	.6	.5	.4	.3	.2	.1	.0
T4EN	–	T4MS1	T4MS0	–	–	T4PAU	T4CC
R/W	–	R/W	R/W	–	–	R/W	R/W

Initial value: 00H

T4EN Control Timer 4

0 Timer 4 disable

1 Timer 4 enable (Counter clear and start)

T4MS[1:0] Control Timer 4 Operation Mode

T4MS1	T4MS0	description
0	0	Timer/counter mode (T4O: toggle at A match)
0	1	Capture mode (The A match interrupt can occur)
1	0	PPG one-shot mode (PWM4O)
1	1	PPG repeat mode (PWM4O)

T4PAU Timer 4 Counter Temporary Pause Control

0 Continue counting

1 Temporary pause

T4CC Clear Timer 4 Counter

0 No effect

1 Clear the Timer 4 counter (When write, automatically cleared “0” after being cleared counter)

T4CRL (Timer 4 Control Low Register) : C8H

.7	.6	.5	.4	.3	.2	.1	.0
T4CK2	T4CK1	T4CK0	T4IFR	RLD4EN	T4POL	T4ECE	T4CNTR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

T4CK[2:0] Select Timer 4 clock source. fx is system clock frequency

T4CK2	T4CK1	T4CK0	description
0	0	0	fx/512
0	0	1	fx/32
0	1	0	fx/16
0	1	1	fx/8
1	0	0	fx/4
1	0	1	fx/2
1	1	0	fx/1
1	1	1	External clock (EC4)

T4IFR When T4 Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 T4 Interrupt no generation

1 T4 Interrupt generation

RLD4EN Control Timer 4 Reload Signal

0 Enable Timer 4 reload signal

1 Disable Timer 4 reload signal

T4POL T4O/PWM4O Polarity Selection

0 Start High (T4O/PWM4O is low level at disable)

1 Start Low (T4O/PWM4O is high level at disable)

T4ECE Timer 4 External Clock Edge Selection

0 External clock falling edge

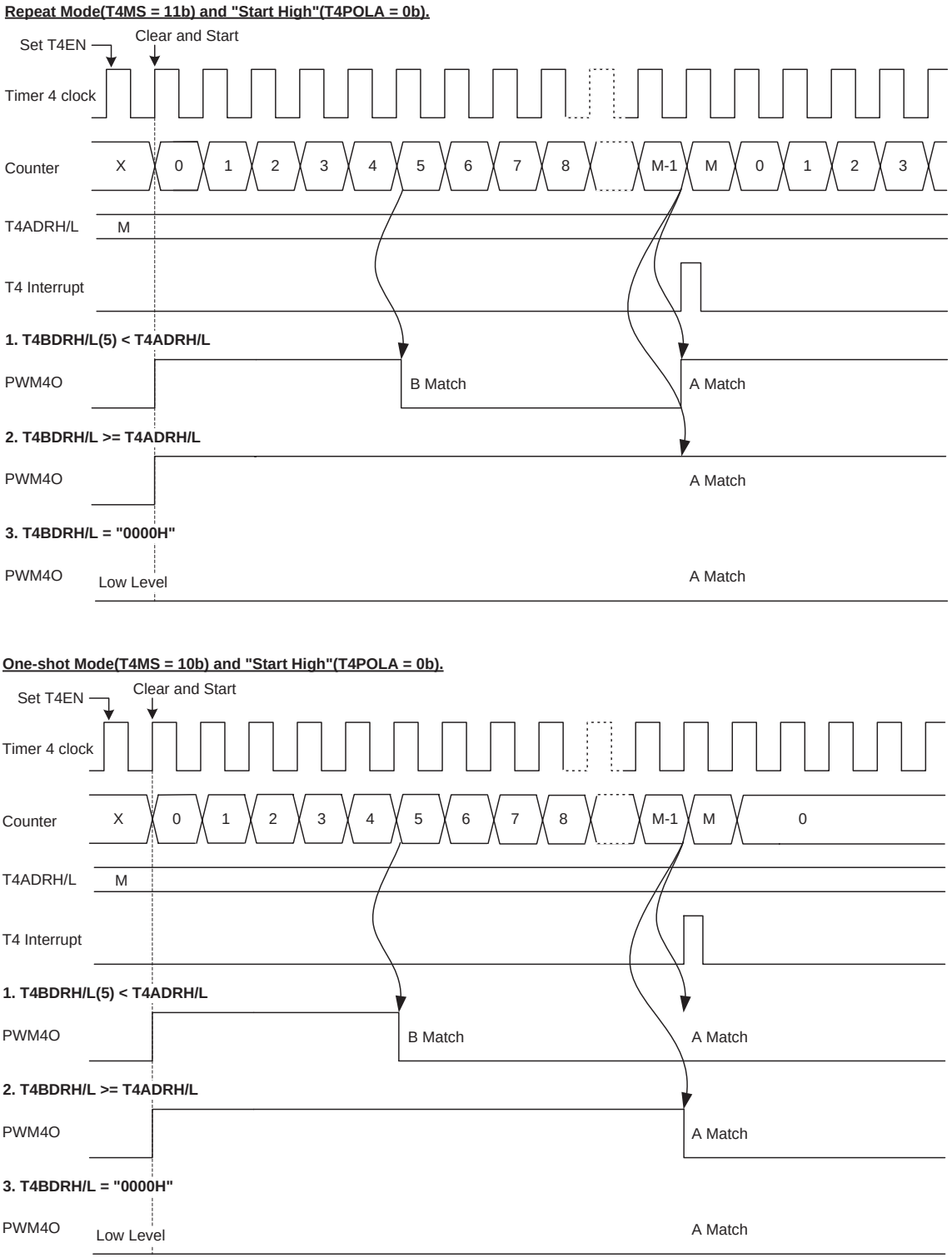
1 External clock rising edge

T4CNTR Timer 4 Counter Read Control

0 No effect

1 Load the counter value to the B data register (When write, automatically cleared “0” after being loaded)

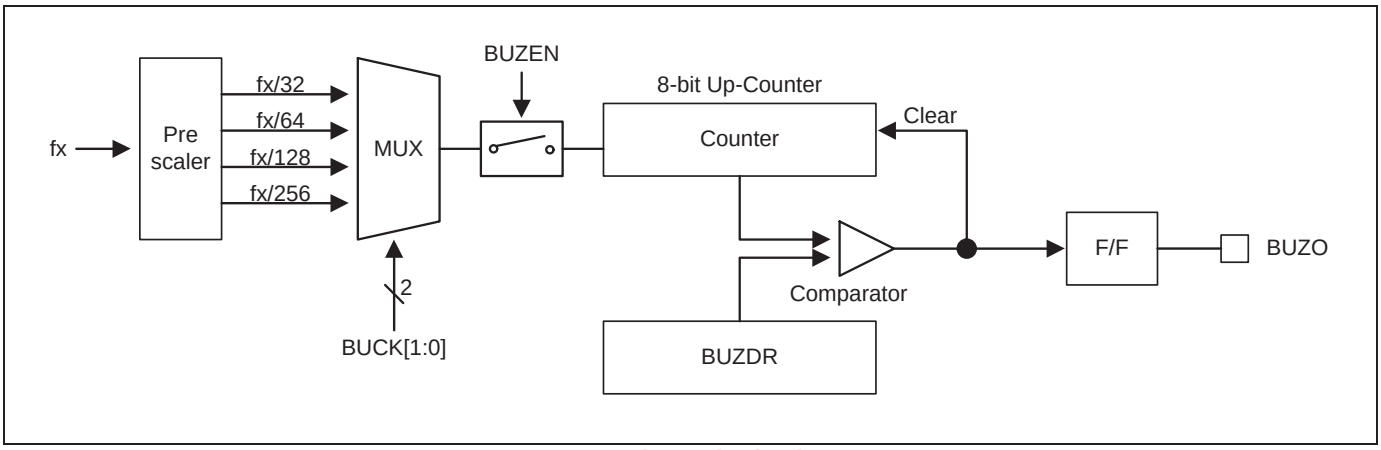
10.7.4 TIMER 4 PPG MODE TIMING CHART



PPG Mode Timing Chart

10.8 BUZZER DRIVER

10.8.1 BLOCK DIAGRAM



BUZZER Driver Block Diagram

10.8.2 REGISTER MAP

Name	Address	Dir	Default	Description
BUZDR	8FH	R/W	FFH	BUZZER Data Register
BUZCR	97H	R/W	00H	BUZZER Control Register

Register Map

10.8.3 REGISTER DESCRIPTION FOR BUZZER DRIVER

BUZDR (Buzzer Data Register) : 8FH

.7	.6	.5	.4	.3	.2	.1	.0
BUZDR7	BUZDR6	BUZDR5	BUZDR4	BUZDR3	BUZDR2	BUZDR1	BUZDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

BUZDR[7:0] This bits control the BUZZER frequency.
Its resolution is 00H to FFH.

BUZCR (BUZZER Control Register) : 97H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	–	BUCK1	BUCK0	BUZEN
–	–	–	–	–	R/W	R/W	R/W

Initial value: 00H

BUCK[1:0] BUZZER driver source clock selection

BUCK1	BUCK0	description
0	0	fx/32
0	1	fx/64
1	0	fx/128
1	1	fx/256

BUZEN BUZZER driver operation Control

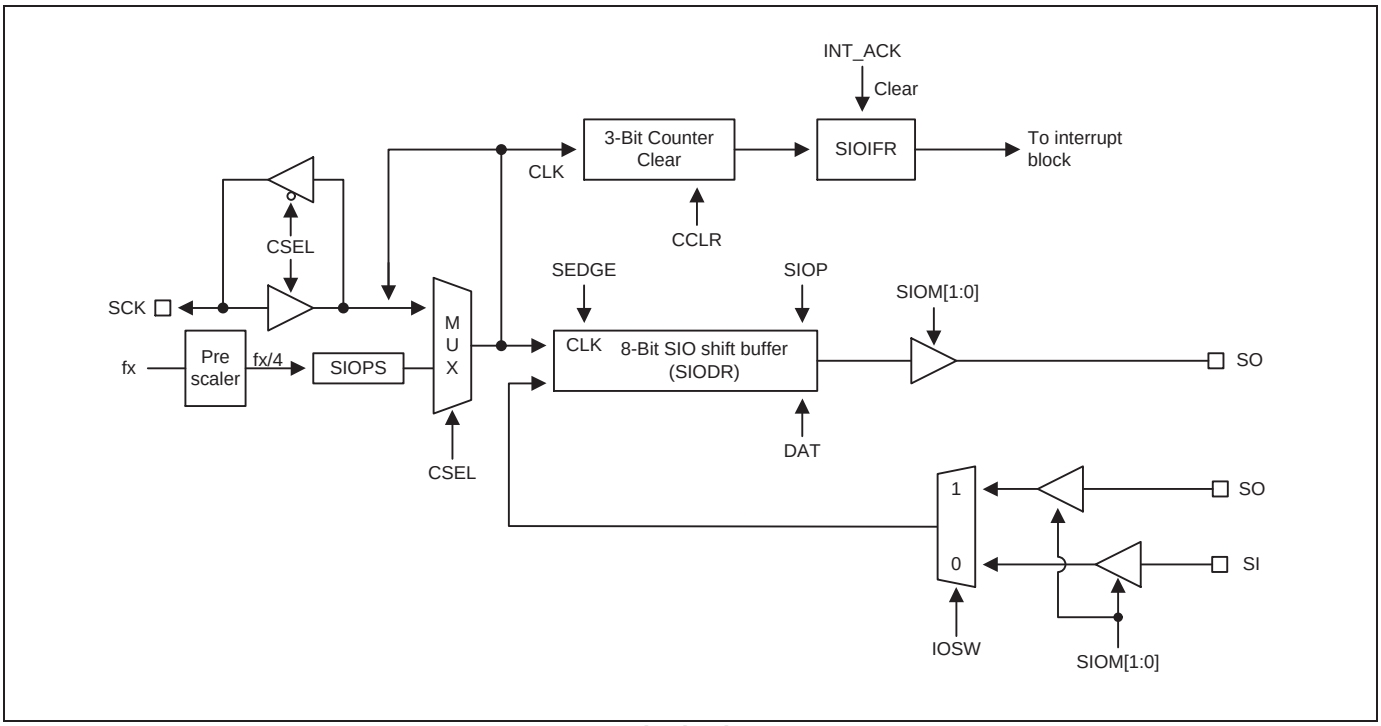
0 BUZZER driver disable

1 BUZZER driver enable

Note: fx = System clock frequency

10.9 SERIAL I/O

10.9.1 BLOCK DIAGRAM



SIO Block Diagram

10.9.2 REGISTER MAP

Name	Address	Dir	Default	Description
SIOPS	B7H	R/W	00H	SIO Pre-scaler Register
SIODR	B6H	R/W	00H	SIO Data Register
SIOCR	B5H	R/W	00H	SIO Control Register

Register Map

10.9.3 REGISTER DESCRIPTION FOR SIO

SIOPS (SIO Pre-Scaler Register) : B7H

.7	.6	.5	.4	.3	.2	.1	.0
SIOPS7	SIOPS6	SIOPS5	SIOPS4	SIOPS3	SIOPS2	SIOPS1	SIOPS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

SIOPS[7:0] SIO Pre-Scaler

Baud Rate = (fx/4)/(SIOPS+1)

SIODR (SIO Data Register) : B6H

.7	.6	.5	.4	.3	.2	.1	.0
SIODR7	SIODR6	SIODR5	SIODR4	SIODR3	SIODR2	SIODR1	SIODR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

SIODR[7:0] SIO Data

SIOCR (SIO Control Register) : B5H

.7	.6	.5	.4	.3	.2	.1	.0
CSEL	DAT	SIOP	IOSW	SIOM1	SIOM0	CCLR	SEDGE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

CSEL SIO Shift Clock Selection

0 Internal clock (P.S clock)

1 External clock (SCK)

DAT Data Direction Control

0 MSB first mode

1 LSB first mode

SIOP SIO Shift Operation Enable

0 Disable shifter and clock counter

1 Enable shifter and clock counter

IOSW Serial Input Pin Selection bit

0 SI pin selection

1 SO pin selection

Note: If the SO pin is selected for a serial data input, the SO pin should be set to an input and port. So, the SIOM, P5FSRH.6-.5 and P57IO bits should be set to '01b', '00b' and '0b', respectively. Refer to the P5IO and P5FSRH registers for setting.

SIOM[1:0] SIO Mode Selection

SIOM1	SIOM0	description
0	0	Transmit mode
0	1	Receive mode
1	X	Transmit/Receive mode

CCLR SIO Counter Clear and Shift Start

0 No action

1 Clear 3-bit counter and start shifting

SEDGE SIO Clock Edge Selection

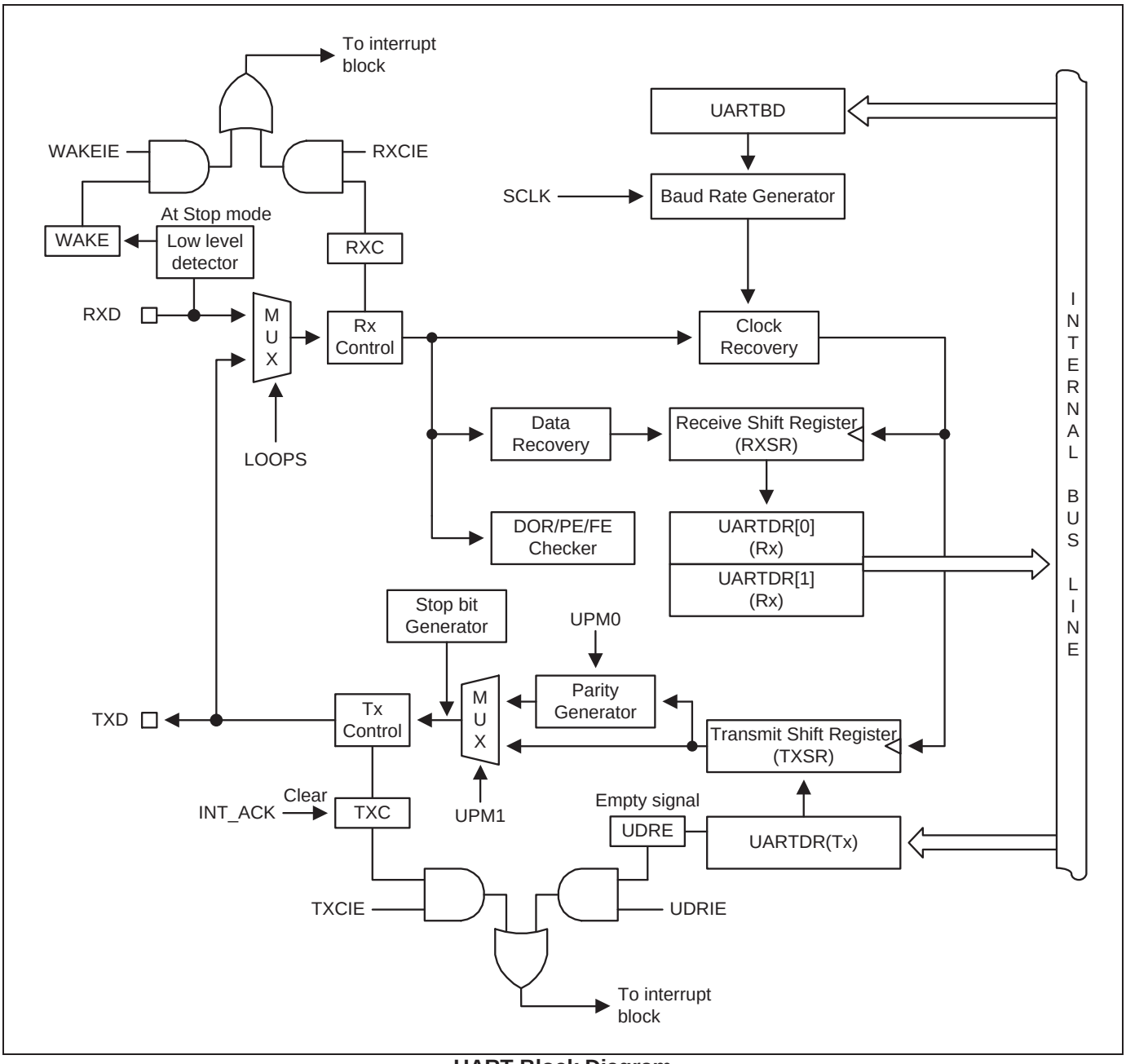
0 Tx at falling edges, Rx at rising edges

1 Tx at rising edges, Rx at falling edges

Note: The serial I/O interrupt flag (SIOIFR bit) is in the timer interrupt flag register (TIFR register).

10.10 UART

10.10.1 BLOCK DIAGRAM



UART Block Diagram

10.10.2 REGISTER MAP

Name	Address	Dir	Default	Description
UARTCR1	E2H	R/W	00H	UART Control Register 1
UARTCR2	E3H	R/W	00H	UART Control Register 2
UARTCR3	E4H	R/W	00H	UART Control Register 3
UARTST	E5H	R/W	80H	UART Status Register
UARTBD	E6H	R/W	FFH	UART Baud Rate Generation Register
UARTDR	EFH	R/W	00H	UART Data Register

Register Map

10.10.3 REGISTER DESCRIPTION FOR UART

UARTBD (UART Baud-Rate Generation Register) : E6H

.7	.6	.5	.4	.3	.2	.1	.0
UARTBD7	UARTBD6	UARTBD5	UARTBD4	UARTBD3	UARTBD2	UARTBD1	UARTBD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

UARTBD[7:0] The value in this register is used to generate internal baud rate. To prevent malfunction, do not write ‘0’.

UARTDR (UART Data Register) : E7H

.7	.6	.5	.4	.3	.2	.1	.0
UARTDR7	UARTDR6	UARTDR5	UARTDR4	UARTDR3	UARTDR2	UARTDR1	UARTDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

UARTDR[7:0] The UART Transmit buffer and Receive buffer share the same I/O address with this DATA register. The Transmit Data Buffer is the destination for data written to the UARTDR register. Reading the UARTDR register returns the contents of the Receive Buffer. Write this register only when the UDRE flag is set.

UARTCR1 (UART Control Register 1) : E2H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	UPM1	UPM0	USIZE2	USIZE1	USIZE0	–
–	–	R/W	R/W	R/W	R/W	R/W	–

Initial value: 00H

UPM[1:0] Selects Parity Generation and Check methods

UPM1	UPM0	Parity
0	0	No Parity
0	1	Reserved
1	0	Even Parity
1	1	Odd Parity

USIZE[2:0] Selects the length of bits in frame.

USIZE2	USIZE1	USIZE0	Data Length
0	0	0	5 bit
0	0	1	6 bit
0	1	0	7 bit
0	1	1	8 bit
1	1	1	9 bit
Other values:			Reserved

UARTCR2 (UART Control Register 2) : E3H

.7	.6	.5	.4	.3	.2	.1	.0
UDRIE	TXCIE	RXCIE	WAKEIE	TXE	RXE	UARTEN	U2X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

UDRIE Interrupt enable bit for UART Data Register Empty.

0 Interrupt from UDRE is inhibited (use polling)

1 When UDRE is set, request an interrupt

TXCIE Interrupt enable bit for Transmit Complete.

0 Interrupt from TXC is inhibited (use polling)

1 When TXC is set, request an interrupt

RXCIE Interrupt enable bit for Receive Complete.

0 Interrupt from RXC is inhibited (use polling)

1 When RXC is set, request an interrupt

WAKEIE Interrupt enable bit for Wake in STOP mode. When device is in stop mode, if RXD goes to Low level an interrupt can be requested to wake-up system. At that time the UDRIE bit and UARTST register value should be set to ‘0b’ and “00H”, respectively.

0 Interrupt from Wake is inhibited

1 When WAKE is set, request an interrupt

TXE Enables the Transmitter unit.

0 Transmitter is disabled

1 Transmitter is enabled

RXE Enables the Receiver unit.

0 Receiver is disabled

1 Receiver is enabled

UARTEN Activate UART module by supplying clock. When one of TXE and RXE values is “1”, the UARTEN bit always set to “1”.

0 UART is disabled (clock is halted)

1 UART is enabled

U2X This bit selects receiver sampling rate.

0 Normal operation

1 Double speed operation

UARTCR3 (UART Control Register 3) : E4H

.7	.6	.5	.4	.3	.2	.1	.0
–	LOOPS	–	–	–	USBS	TX8	RX8
–	R/W	–	–	–	R/W	R/W	R/W

Initial value: 00H

LOOPS Control the Loop Back mode of UART, for test mode.

0 Normal operation

1 Loop Back mode

USBS Selects the length of stop bit.

0 1 Stop bit

1 2 Stop bit

TX8 The ninth bit of data frame in UART. Write this bit first before loading the UARTDR register.

0 MSB (9^{th} bit) to be transmitter is ‘0’

1 MSB (9^{th} bit) to be transmitter is ‘1’

RX8 The ninth bit of data frame in UART. Read this bit first before reading the receive buffer.

0 MSB (9^{th} bit) to be received is ‘0’

1 MSB (9^{th} bit) to be received is ‘1’

UARTST (UART Status Register) : E5H

.7	.6	.5	.4	.3	.2	.1	.0
UDRE	TXC	RXC	WAKE	SOFTRST	DOR	FE	PE
R/W	R/W	R	R/W	R/W	R	R/W	R/W

Initial value: 80H

UDRE The UDRE flag indicates if the transmit buffer (UARTDR) is ready to receive new data. If UDRE is '1', the buffer is empty and ready to be written. The flag can generate a UDRE interrupt.

0 Transmit buffer is not empty

1 Transmit buffer is empty

TXC This flag is set when the entire frame in the transmit shift register has been shifted out and there is no new data currently present in the transmit buffer. This flag is automatically cleared when the interrupt service routine of a TXC interrupt is executed. This flag can generate a TXC interrupt. This bit is auto cleared.

0 Transmission is ongoing

1 Transmit buffer is empty and the data in transmit shift register are shifted out completely

RXC This flag is set when there are unread data in the receive buffer and cleared when all the data in the receive buffer are read. The RXC flag can be used to generate a RXC interrupt. This bit is auto cleared.

0 There is no data unread in the receive buffer

1 There are more than 1 data in the receive buffer

WAKE This flag is set when the RXD pin is detected low while the CPU is in STOP mode. This flag can be used to generate a WAKE interrupt. This bit should be cleared by program software.

0 No WAKE interrupt is generated

1 WAKE interrupt is generated

SOFTRST This is an internal reset and only has effect on UART. Writing '1' to this bit initializes the internal logic of UART and is auto cleared.

0 No operation

1 Reset UART

DOR This bit is set if data OverRun occurs. While this bit is set, the incoming data frame is ignored. This flag is valid until the receive buffer is read.

0 No Data OverRun

1 Data OverRun detected

FE This bit is set if the first stop bit of next character in the receive buffer is detected as ‘0’. This bit is valid until the receive buffer is read.

0 No Frame Error

1 Frame Error detected

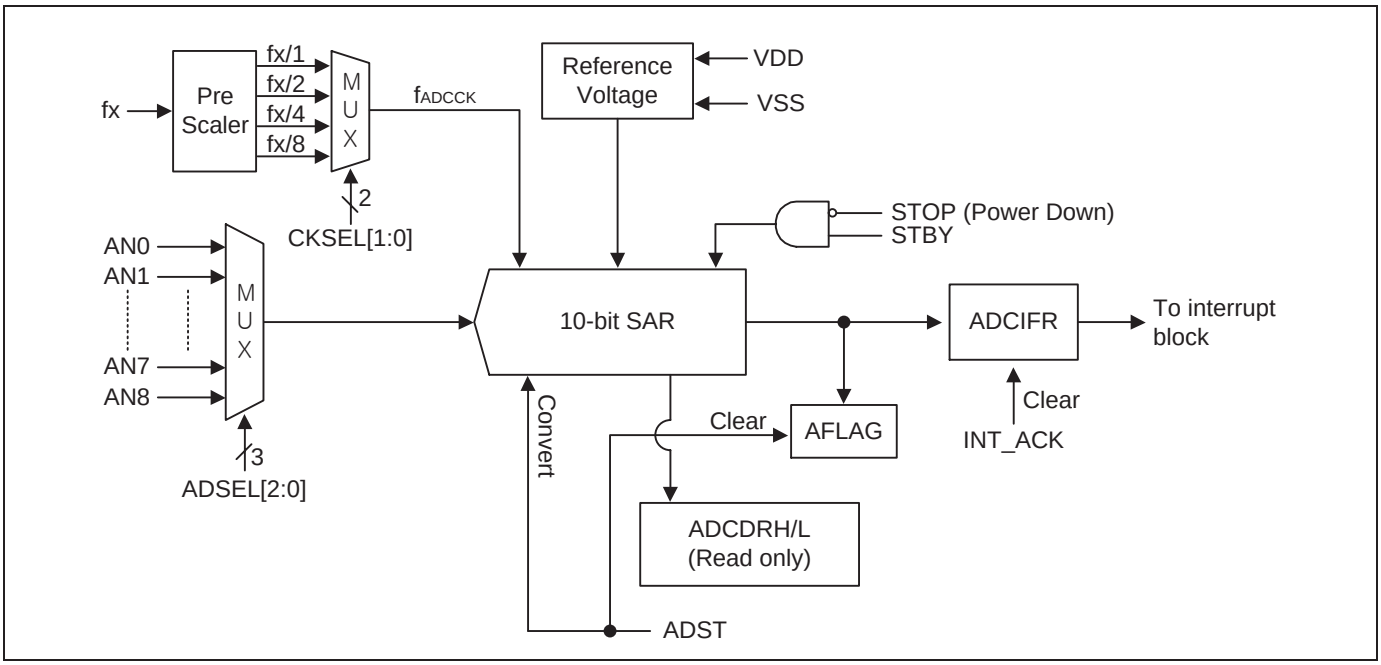
PE This bit is set if the next character in the receive buffer has a Parity Error when received while Parity Checking is enabled. This bit is valid until the receive buffer is read.

0 No Parity Error

1 Parity Error detected

10.11 10-BIT A/D CONVERTER

10.11.1 BLOCK DIAGRAM



10-bit A/D Converter Block Diagram

10.11.2 REGISTER MAP

Name	Address	Dir	Default	Description
ADCCRH	9DH	R/W	00H	A/D Converter Control High Register
ADCCRL	9CH	R/W	00H	A/D Converter Control Low Register
ADCDRH	A7H	R	xxH	A/D Converter Data High Register
ADCDRL	A6H	R	xxH	A/D Converter Data Low Register

Register Map

10.11.3 REGISTER DESCRIPTION FOR A/D CONVERTER

ADCDRH (A/D Converter Data High Register) : A7H

.7	.6	.5	.4	.3	.2	.1	.0
ADDM9	ADDM8	ADDM7	ADDM6	ADDM5	ADDM4	ADDM3 ADDL9	ADDM2 ADDL8
R	R	R	R	R	R	R	R

Initial value: xxH

ADDM[9:2] MSB align, A/D Converter High Result (8bit)

ADDL[9:8] LSB align, A/D Converter High Result (2bit)

ADCDRL (A/D Converter Data Low Register) : A6H

.7	.6	.5	.4	.3	.2	.1	.0
ADDM1 ADDL7	ADDM0 ADDL6	ADDL5	ADDL4	ADDL3	ADDL2	ADDL1	ADDL0
R	R	R	R	R	R	R	R

Initial value: xxH

ADDM[1:0] MSB align, A/D Converter Low Result (2bit)

ADDL[7:0] LSB align, A/D Converter Low Result (8bit)

ADCCRH (A/D Converter Control High Register) : 9DH

.7	.6	.5	.4	.3	.2	.1	.0
ADCIFR	–	–	–	–	ALIGN	CKSEL1	CKSEL0
R/W	–	–	–	–	R/W	R/W	R/W

Initial value: 00H

ADCIFR When ADC Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.

0 ADC Interrupt no generation

1 ADC Interrupt generation

ALIGN A/D Converter Data Align Selection

0 MSB align; ADCDRH[7:0], ADCDRL[7:6]

1 LSB align; ADCDRH[1:0], ADCDRL[7:0]

CKSEL[1:0] A/D Converter Clock Selection

CKSEL1	CKSEL0	description
0	0	fx/1
0	1	fx/2
1	0	fx/4
1	1	fx/8

ADCCRL (A/D Converter Control Low Register) : 9CH

.7	.6	.5	.4	.3	.2	.1	.0
STBY	ADST	–	AFLAG	–	ADSEL2	ADSEL1	ADSEL0
R/W	R/W	–	R	–	R/W	R/W	R/W

Initial value: 00H

STBY Control operation of A/DC
(The ADC module is automatically disabled at stop mode)

0 ADC module disable

1 ADC module enable

ADST Control A/D Conversion Start

0 No effect

1 Trigger signal generation for conversion start

AFLAG A/D Converter Operation State (This bit is cleared to '0' when the STBY bit is set to '0' or when the CPU is at stop mode)

0 During A/D Conversion

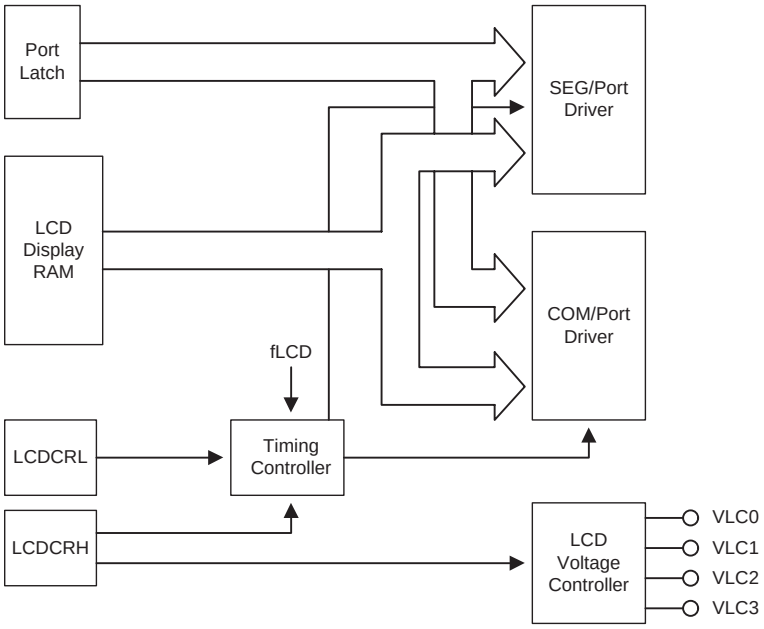
1 A/D Conversion finish

ADSEL[2:0] A/D Converter Channel Selection

ADSEL2	ADSEL1	ADSEL0	description
0	0	0	AN0
0	0	1	AN1
0	1	0	AN2
0	1	1	AN3
1	0	0	AN4
1	0	1	AN5
1	1	0	AN6
1	1	1	AN7

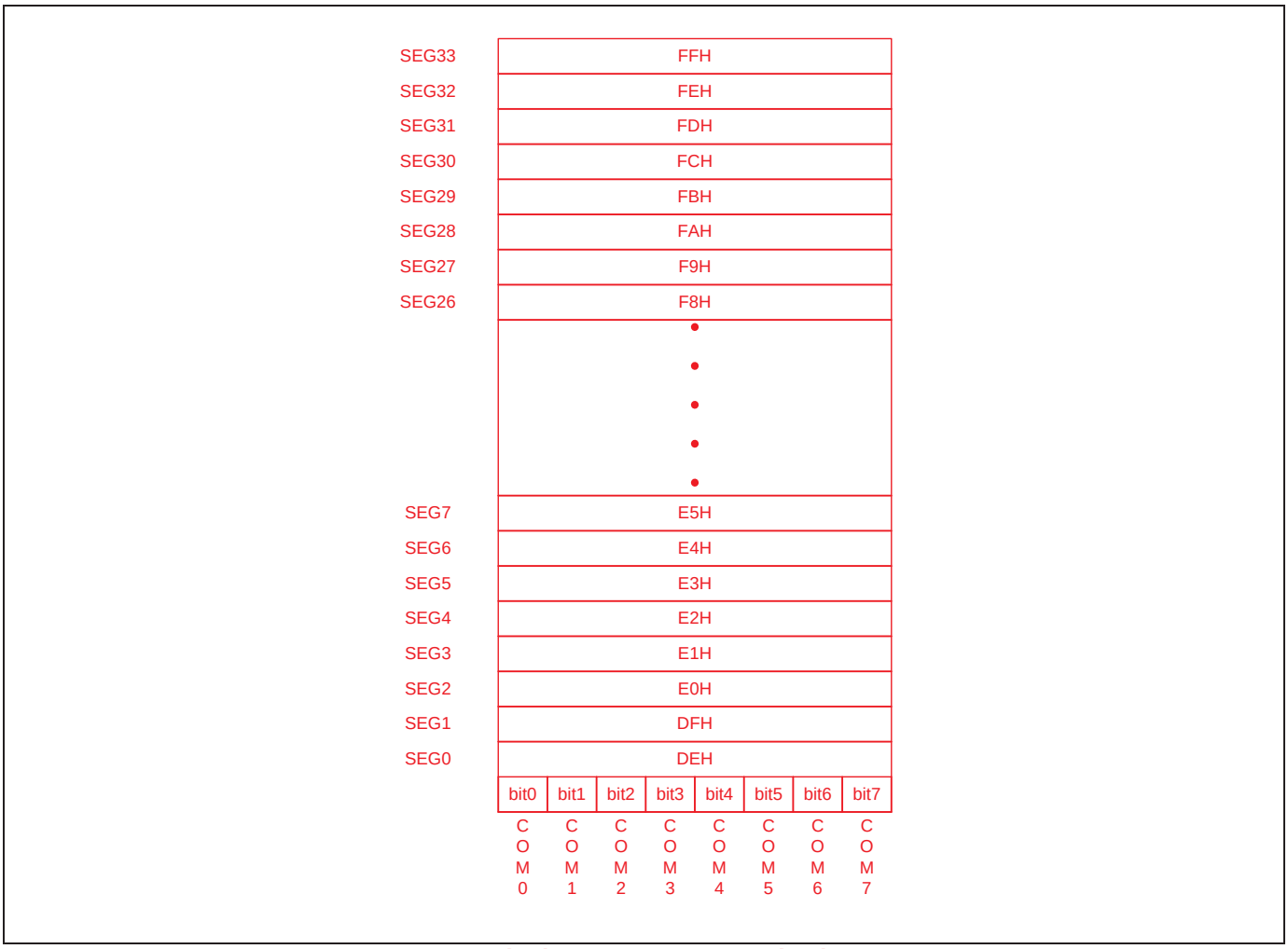
10.12 LCD DRIVER

10.12.1 BLOCK DIAGRAM



LCD Circuit Diagram

10.12.2 LCD DISPLAY RAM ORGANIZATION



LCD Display Data Ram Organization

10.12.3 REGISTER MAP

Name	Address	Dir	Default	Description
LCDCCR	F5H	R/W	00H	LCD Contrast Control Register
LCDCRH	ECH	R/W	00H	LCD Driver Control High Register
LCDCRL	EBH	R/W	00H	LCD Driver Control Low Register

Register Map

10.12.4 REGISTER DESCRIPTION FOR LCD DRIVER

LCDCRH (LCD Driver Control High Register) : ECH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	–	–	–	DISP
–	–	–	–	–	–	–	R/W

Initial value: 00H

DISP LCD Display Control

0 Display off

1 Normal display on

LCDCRL (LCD Driver Control Low Register) : EBH

.7	.6	.5	.4	.3	.2	.1	.0
IRSEL1	IRSEL0	DBS3	DBS2	DBS1	DBS0	LCLK1	LCLK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

IRSEL Internal LCD Bias Dividing Resistor Select

IRSEL1	IRSEL0	
0	0	R_{LCD} = 60kΩ (R_{LCD2})
0	1	R_{LCD} = 30kΩ (R_{LCD1})
1	0	R_{LCD} = 120kΩ (R_{LCD3})
1	1	Not available

DBS[3:0] LCD Duty and Bias Select

DBS3	DBS2	DBS1	DBS0	description
0	0	0	0	1/8 duty, 1/4 bias, R_{LCD}
0	0	0	1	1/6 duty, 1/4 bias, R_{LCD}
0	0	1	0	1/5 duty, 1/3 bias, R_{LCD}
0	0	1	1	1/4 duty, 1/3 bias, R_{LCD}
0	1	0	0	1/3 duty, 1/3 bias, R_{LCD}
0	1	0	1	1/3 duty, 1/2 bias, R_{LCD}
0	1	1	0	1/3 duty, 1/2 bias, 2xR_{LCD}
0	1	1	1	1/2 duty, 1/2 bias, R_{LCD}
1	0	0	0	1/2 duty, 1/2 bias, 2xR_{LCD}
Other value				Not available

LCLK[1:0] LCD Clock Select (When fwck(Watch timer clock)=32.768kHz)

LCLK1	LCLK0	description
0	0	fLCD = 128Hz
0	1	fLCD = 256Hz
1	0	fLCD = 512Hz
1	1	fLCD = 1024Hz

Note: The LCD clock is generated by watch timer clock (f_{WCK}). So the watch timer should be enabled when the LCD display is turned on.

LCDCCR (LCD Driver Contrast Control Register) : F5H

.7	.6	.5	.4	.3	.2	.1	.0
LCTEN	–	–	–	VLCD3	VLCD2	VLCD1	VLCD0
R/W	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

LCTEN Control LCD Driver Contrast

0 LCD Driver Contrast disable

1 LCD Drive Contrast enable

VLCD[3:0] VLC0 Voltage Control when the contrast is enabled

VLCD3	VLCD2	VLCD1	VLCD0	description
0	0	0	0	VLC0 = VDD x 16/31 step
0	0	0	1	VLC0 = VDD x 16/30 step
0	0	1	0	VLC0 = VDD x 16/29 step
0	0	1	1	VLC0 = VDD x 16/28 step
0	1	0	0	VLC0 = VDD x 16/27 step
0	1	0	1	VLC0 = VDD x 16/26 step
0	1	1	0	VLC0 = VDD x 16/25 step
0	1	1	1	VLC0 = VDD x 16/24 step
1	0	0	0	VLC0 = VDD x 16/23 step
1	0	0	1	VLC0 = VDD x 16/22 step
1	0	1	0	VLC0 = VDD x 16/21 step
1	0	1	1	VLC0 = VDD x 16/20 step
1	1	0	0	VLC0 = VDD x 16/19 step
1	1	0	1	VLC0 = VDD x 16/18 step
1	1	1	0	VLC0 = VDD x 16/17 step
1	1	1	1	VLC0 = VDD x 16/16 step

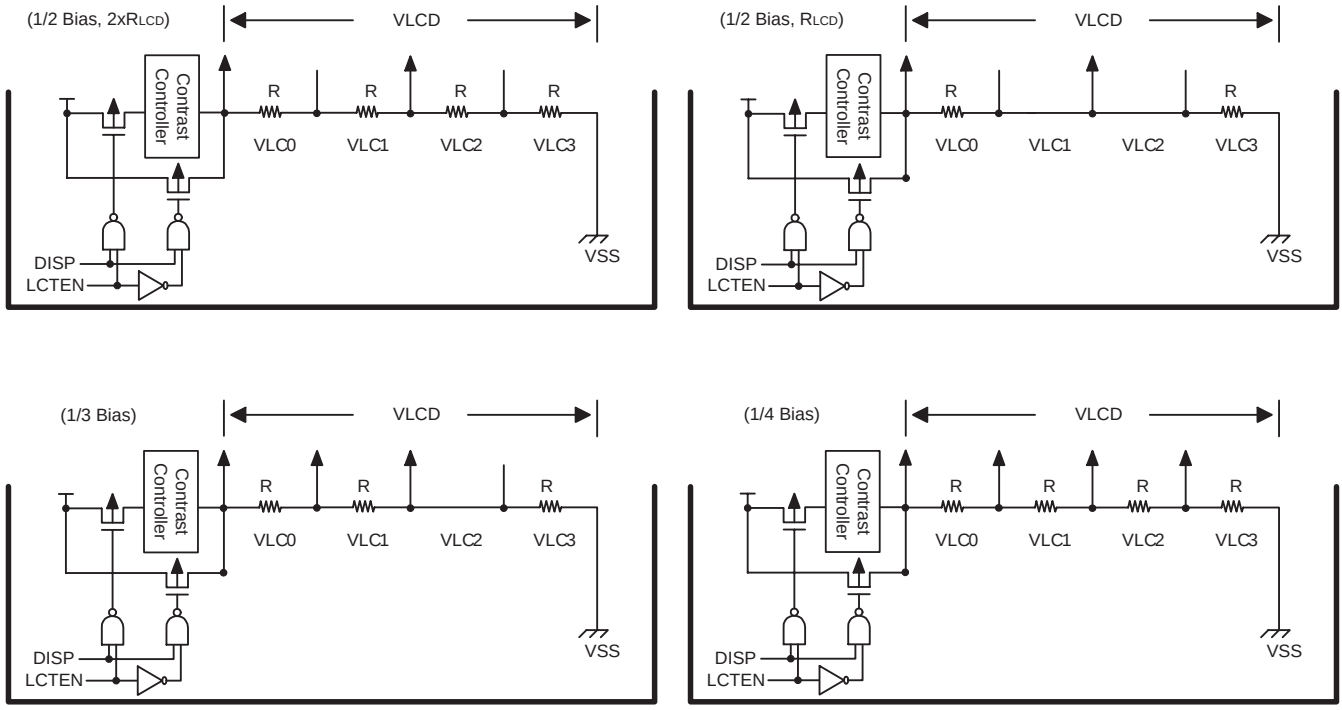
Note: The contrast step is based on 1/4 bias and R_{LCD} = 60kΩ.

1/4 bias: VDD x 8/(23 – VLCD[3:0]) when R_{LCD} = 30kΩ
VDD x 16/(31 – VLCD[3:0]) when R_{LCD} = 60kΩ
VDD x 32/(47 – VLCD[3:0]) when R_{LCD} = 120kΩ

1/3 bias: VDD x 6/(21 – VLCD[3:0]) when R_{LCD} = 30kΩ
VDD x 12/(27– VLCD[3:0]) when R_{LCD} = 60kΩ
VDD x 24/(39– VLCD[3:0]) when R_{LCD} = 120kΩ

1/2 bias: VDD x 4/(21 – VLCD[3:0]) when R_{LCD} = 30kΩ
VDD x 8/(23 – VLCD[3:0]) when R_{LCD} = 60kΩ
VDD x 16/(31 – VLCD[3:0]) when R_{LCD} = 120kΩ

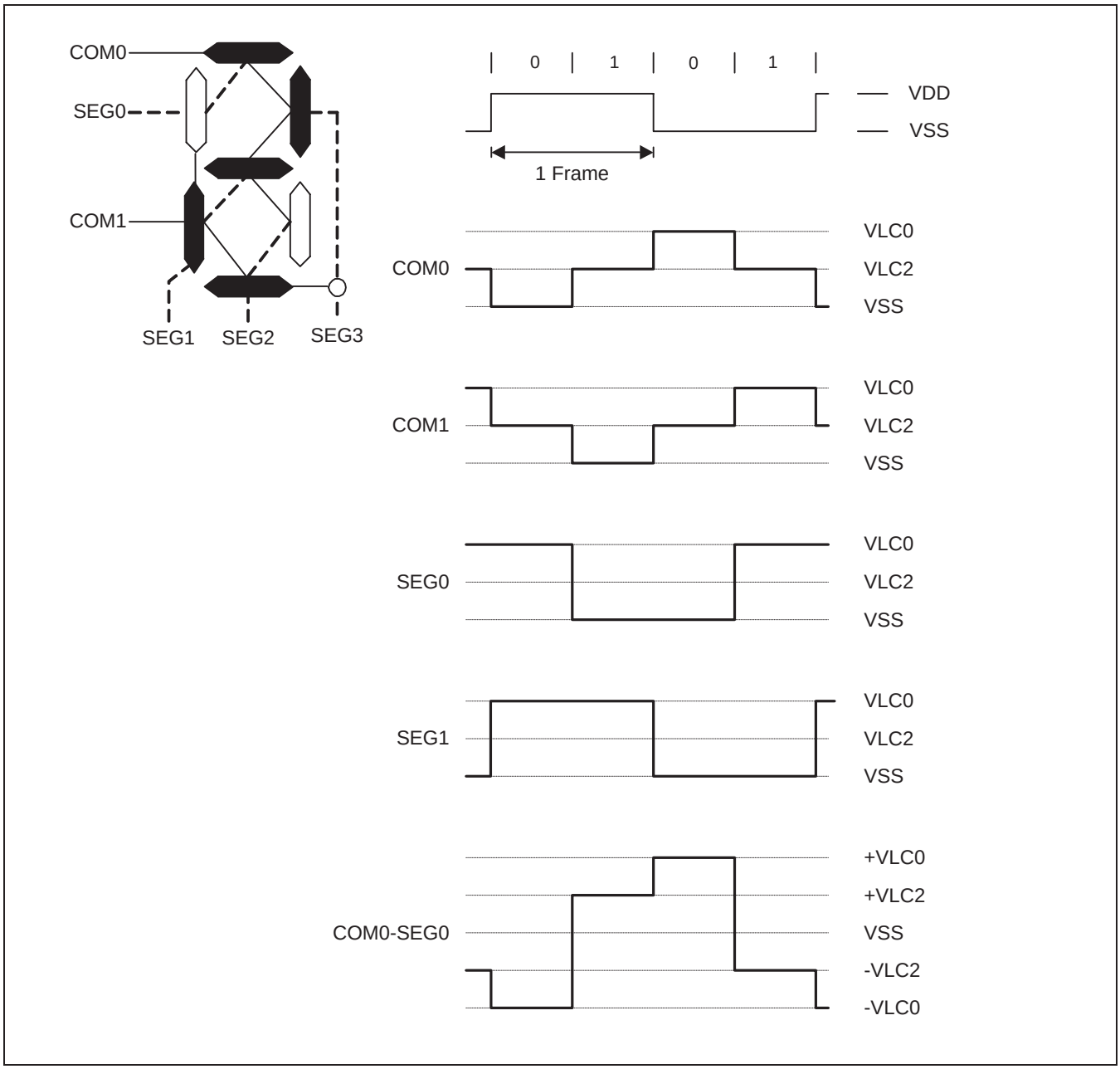
10.12.5 INTERNAL RESISTOR BIAS CONNECTON



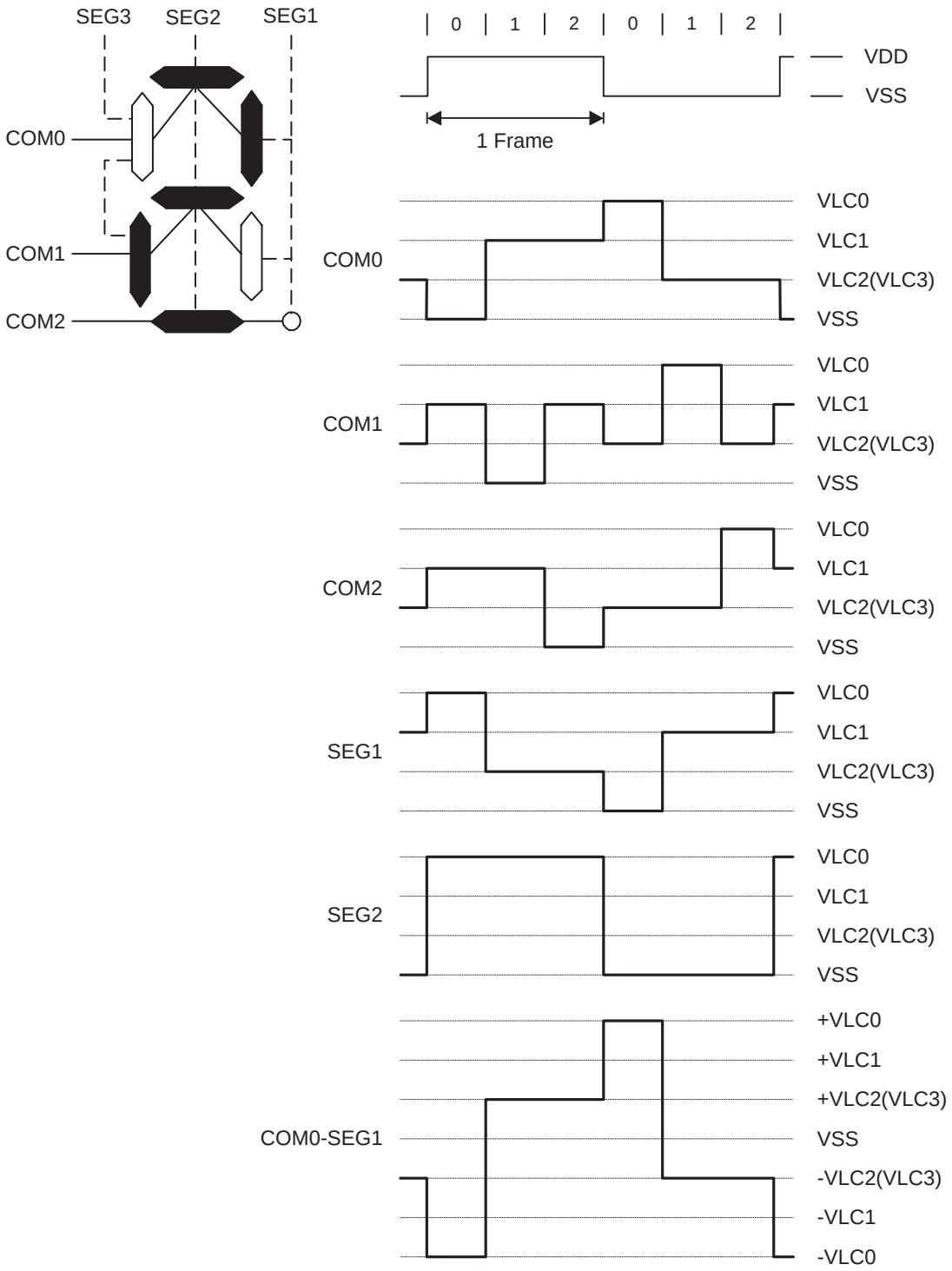
Notes:

1. When 1/2 bias are selected, the VLC0, VLC1 and VLC2, VLC3 are internally connected.
2. When 1/3 bias are selected, the VLC2 and VLC3 are internally connected.

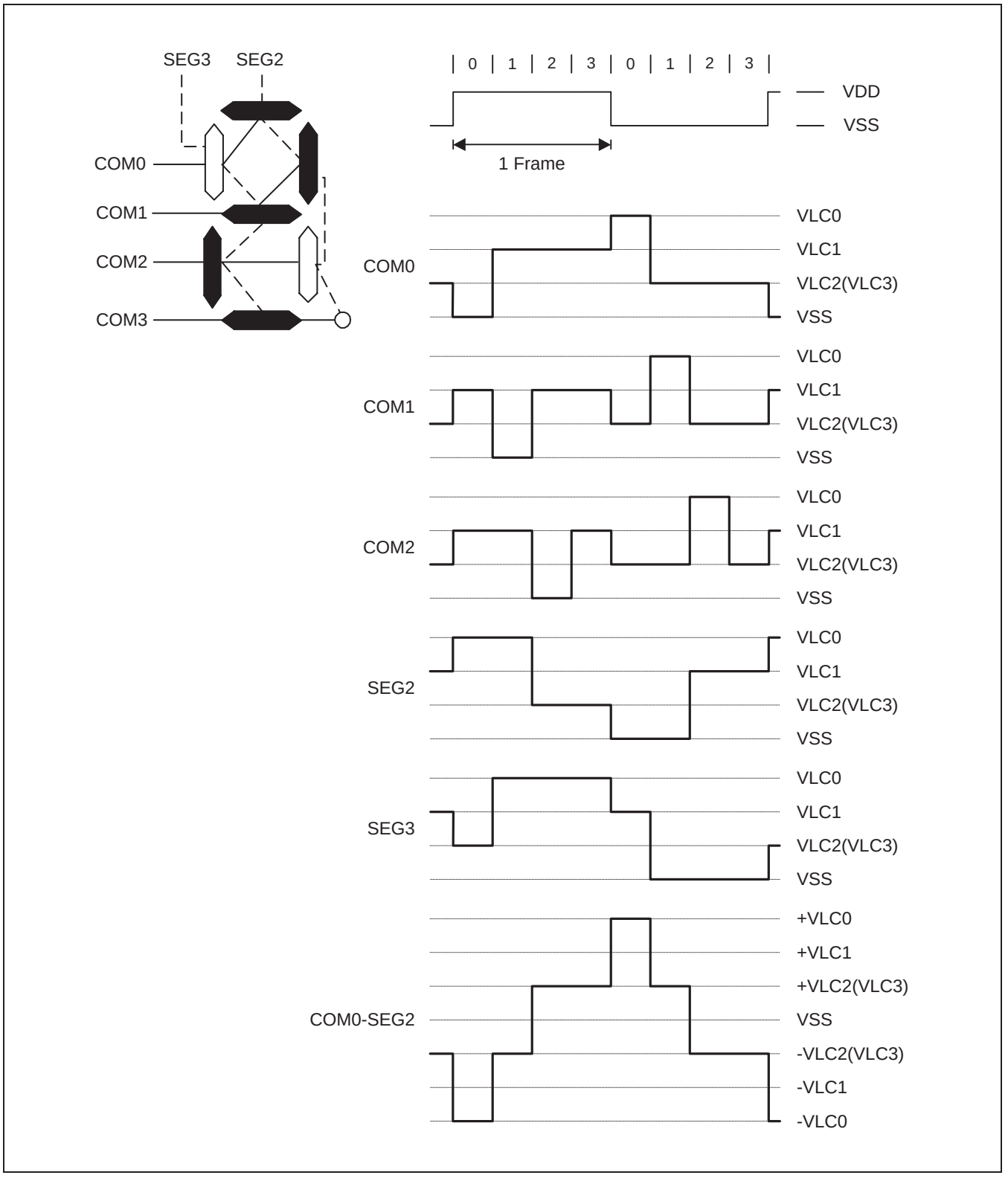
Internal Resistor Bias Connection



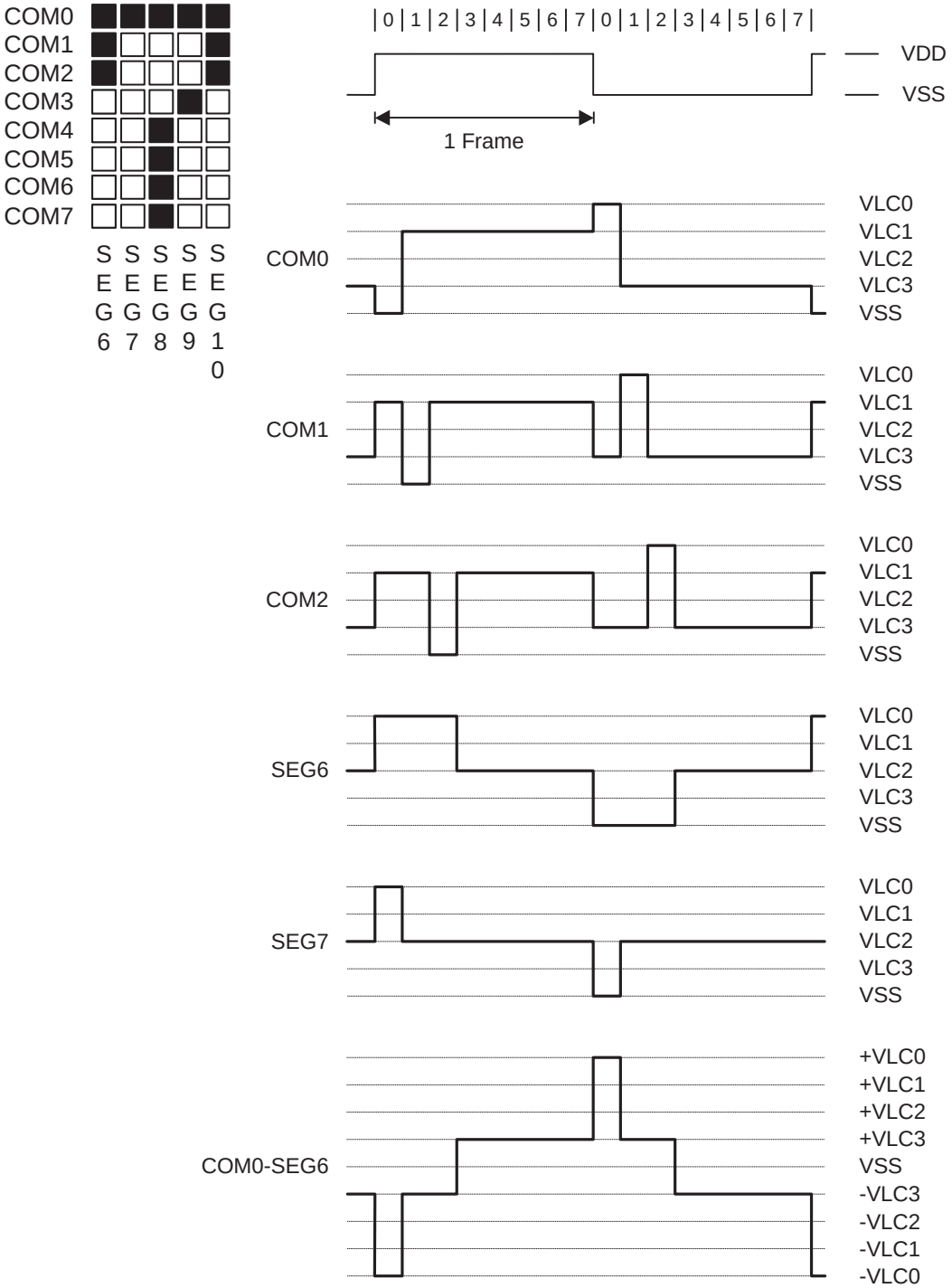
LCD Signal Waveforms (1/2 Duty, 1/2 Bias)



LCD Signal Waveforms (1/3 Duty, 1/3 Bias)



LCD Signal Waveforms (1/4 Duty, 1/3 Bias)



LCD Signal Waveforms (1/8 Duty, 1/4 Bias)

11. Power Down Operation

11.1 POWER DOWN MODE

11.1.1 REGISTER MAP

Name	Address	Dir	Default	Description
RSTFR	86H	R/W	80H	Reset Flag Register
PCON	87H	R/W	00H	Power Control Register
LVRCR	D8H	R/W	00H	Low Voltage Reset Control Register
LVICR	E1H	R/W	00H	Low Voltage Indicator Control Register

Register Map

11.1.2 REGISTER DESCRIPTION

PCON (Power Control Register) : 87H

.7	.6	.5	.4	.3	.2	.1	.0
PCON7	–	–	–	PCON3	PCON2	PCON1	PCON0
R/W	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

PCON[7:0] Power control

01H IDLE mode enable

03H STOP mode enable

Other Values Normal operation

Notes:

1. To enter SLEEP mode, PCON must be set to ‘01H’.
2. To enter STOP mode, PCON must be set to ‘03H’.
3. The PCON register is automatically cleared by a release signal in STOP/SLEEP mode.
4. Three or more NOP instructions must be immediately follow STOP/SLEEP mode like the below example.

```
Ex1)  MOV   PCON, #01H   ; IDLE mode
      NOP
      NOP
      NOP
       •
       •
```

```
Ex2)  MOV   PCON, #03H   ; STOP mode
      NOP
      NOP
      NOP
       •
       •
```

RSTFR (Reset Flag Register) : 86H

.7	.6	.5	.4	.3	.2	.1	.0
PORF	EXTRF	WDTRF	OCDRF	LVRF	–	–	–
R/W	R/W	R/W	R/W	R/W	–	–	–

Initial value: 80H

PORF Power-On Reset flag bit. This bit is reset by writing '0' to this bit.

0 No detection

1 Detection

EXTRF External Reset flag bit. This bit is reset by writing '0' to this bit or by Power-On Reset

0 No detection

1 Detection

WDTRF Watch Dog Reset flag bit. This bit is reset by writing '0' to this bit or by Power-On Reset

0 No detection

1 Detection

OCDRF On-Chip Debug Reset flag bit. This bit is reset by writing '0' to this bit or by Power-On Reset

0 No detection

1 Detection

LVRF Low Voltage Reset flag bit. This bit is reset by writing '0' to this bit or by Power-On Reset

0 No detection

1 Detection

Notes: 1. When the Power-On Reset occurs, the PORF bit is set to "1" and the WDTRF/OCDRF bits are all cleared to "0".
2. When the Power-On Reset occurs, the EXTRF bit is unknown. At that time the EXTRF bit can be set to "1" when External Reset (RESETB) occurs.
3. When the Power-On Reset occurs, the LVRF bit is unknown. At that time the LVRF bit can be set to "1" when LVR Reset occurs.
4. When a reset except the POR occurs, the corresponding flag bit is only set to "1", the other flag bits are kept in the previous.

LVRCR (Low Voltage Reset Control Register) : D8H

.7	.6	.5	.4	.3	.2	.1	.0
LVRST	–	–	LVRVS3	LVRVS2	LVRVS1	LVRVS0	LVREN
R/W	–	–	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

LVRST LVR Enable When Power-down Mode Release

0 Not effect at power-down mode release

1 LVR enable at power-down mode release

Notes:

1. When this bit is ‘1’, the LVREN bit is cleared to ‘0’ by power-down (STOP/IDLE) mode release. (LVR enable)
2. When this bit is ‘0’, the LVREN bit is not effect by power-down mode release.

LVRVS[3:0] LVR Voltage Select

LVRVS3	LVRVS2	LVRVS1	LVRVS0	Description
0	0	0	0	1.60V
0	0	0	1	2.00V
0	0	1	0	2.10V
0	0	1	1	2.20V
0	1	0	0	2.32V
0	1	0	1	2.44V
0	1	1	0	2.59V
0	1	1	1	2.75V
1	0	0	0	2.93V
1	0	0	1	3.14V
1	0	1	0	3.38V
1	0	1	1	3.67V
1	1	0	0	4.00V
1	1	0	1	4.40V
1	1	1	0	Not available
1	1	1	1	Not available

LVREN LVR Operation

0 LVR Enable

1 LVR Disable

Notes:

1. The LVRVS[3:0] bits are cleared by a power-on reset but are retained by other reset signals.
2. The LVRVS[3:0] bits should be set to ‘0000b’ while LVREN bit is “1”

LVICR (Low Voltage Indicator Control Register) : E1H

.7	.6	.5	.4	.3	.2	.1	.0
–	–	LVIF	LVIEN	LVILS3	LVILS2	LVILS1	LVILS0
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

LVIF Low Voltage Indicator flag bit.

0 No detection

1 Detection

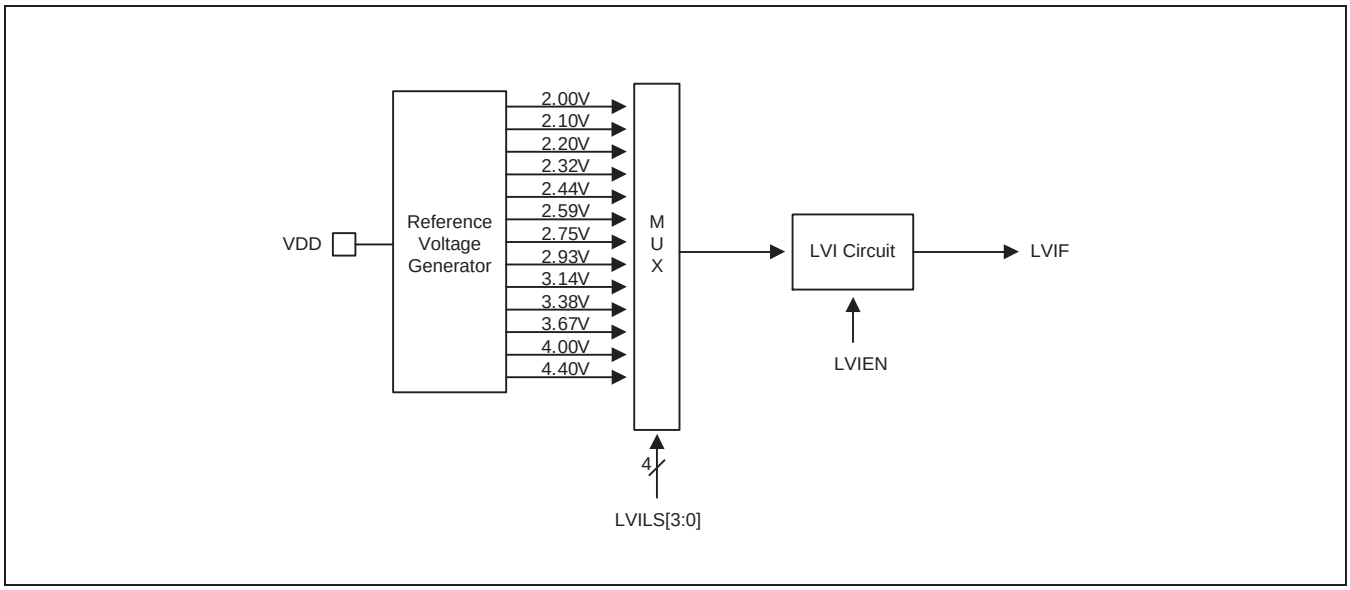
LVIEN LVI Enable/disable

0 Disable

1 Enable

LVILS[3:0] LVI Level Select

LVILS3	LVILS2	LVILS1	LVILS0	Description
0	0	0	0	2.00V
0	0	0	1	2.10V
0	0	1	0	2.20V
0	0	1	1	2.32V
0	1	0	0	2.44V
0	1	0	1	2.59V
0	1	1	0	2.75V
0	1	1	1	2.93V
1	0	0	0	3.14V
1	0	0	1	3.38V
1	0	1	0	3.67V
1	0	1	1	4.00V
1	1	0	0	4.40V
Other Values				Not available



LVI Block Diagram

12. MEMORY PROGRAMMING

12.1 FLASH CONTROL AND STATUS REGISTER

12.1.1 REGISTER MAP

Name	Address	Dir	Default	Description
FSADRH	FAH	R/W	00H	Flash Sector Address High Register
FSADRM	FBH	R/W	00H	Flash Sector Address Middle Register
FSADRL	FCH	R/W	00H	Flash Sector Address Low Register
FIDR	FDH	R/W	00H	Flash Identification Register
FMCR	FEH	R/W	00H	Flash Mode Control Register

Register Map

12.1.2 REGISTER DESCRIPTION

FSADRH (Flash Sector Address High Register) : FAH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	FSADRH3	FSADRH2	FSADRH1	FSADRH0
–	–	–	–	R/W	R/W	R/W	R/W

Initial value: 00H

FSADRH[7:0] Flash Sector Address High

FSADRM (Flash Sector Address Middle Register) : FBH

.7	.6	.5	.4	.3	.2	.1	.0
FSADRM7	FSADRM6	FSADRM5	FSADRM4	FSADRM3	FSADRM2	FSADRM1	FSADRM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

FSADRM[7:0] Flash Sector Address Middle

FSADRL (Flash Sector Address Low Register) : FCH

.7	.6	.5	.4	.3	.2	.1	.0
FSADRL7	FSADRL6	FSADRL5	FSADRL4	FSADRL3	FSADRL2	FSADRL1	FSADRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

FSADRL[7:0] Flash Sector Address Low

FIDR (Flash Identification Register) : FDH

.7	.6	.5	.4	.3	.2	.1	.0
FIDR7	FIDR6	FIDR5	FIDR4	FIDR3	FIDR2	FIDR1	FIDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

FIDR[7:0] Flash Identification

Others No identification value

10100101 Identification value for a flash mode

(These bits are automatically cleared to logic '00H' immediately after one time operation except "flash page buffer reset mode")

FMCR (Flash Mode Control Register) : FEH

.7	.6	.5	.4	.3	.2	.1	.0
FMBUSY	–	–	–	–	FMCR2	FMCR1	FMCR0
R	–	–	–	–	R/W	R/W	R/W

Initial value: 00H

FMBUSY Flash mode busy bit. This bit will be used for only debugger.

0 No effect when "1" is written

1 Busy

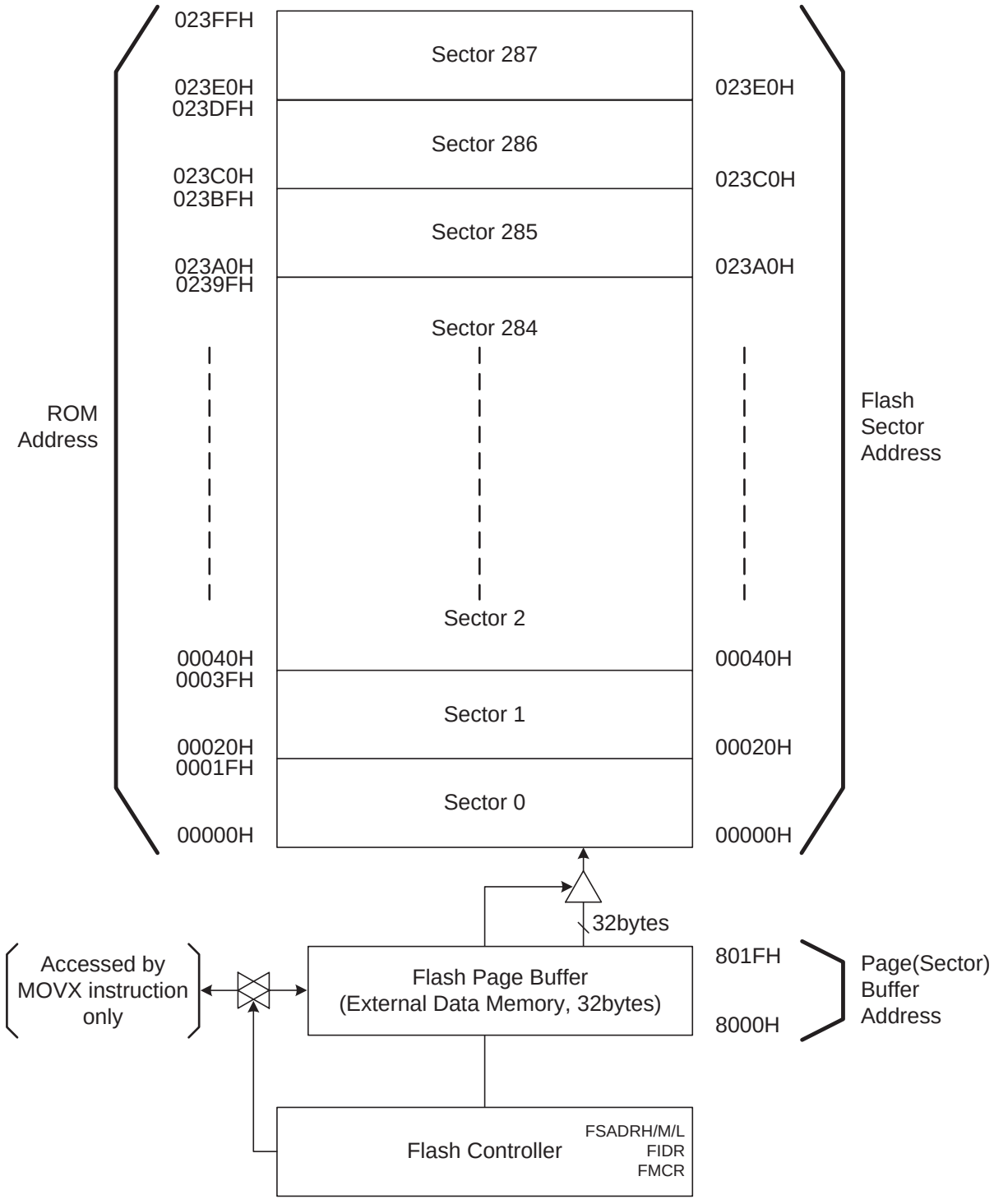
FMCR[2:0] Flash Mode Control Bits. During a flash mode operation, the CPU is hold and the global interrupt is on disable state regardless of the IE.7 (EA) bit.

FMCR2 FMCR1 FMCR Description

0	0	1	Select flash page buffer reset mode and start regardless of the FIDR value (Clear all 32bytes to '0')
0	1	0	Select flash sector erase mode and start operation when the FIDR="10100101b"
0	1	1	Select flash sector write mode and start operation when the FIDR="10100101b"
1	0	0	Select flash hard-lock mode and start operation when the FIDR="10100101b"

Other Values: No operation
(These bits are automatically cleared to logic '00H' immediately after one time operation)

12.2 FLASH PROGRAM ROM STRUCTURE



Note: The corresponding address of flash should be erased to write data on flash.

13. CONFIGURE OPTION

13.1 CONFIGURE OPTION

CONFIGURE OPTION 1 : ROM Address 001EH

.7	.6	.5	.4	.3	.2	.1	.0
–	–	–	–	PAEN	PASS2	PASS1	PASS0

Initial value: 00H

PAEN Protection Area Enable/Disable

0 Disable Protection (Erasable by instruction)

1 Enable Protection (Not erasable by instruction)

PASS[2:0] Protection Area Size Select

PASS2	PASS1	PASSS0	description
0	0	0	0.7K Bytes (0100h – 03FFH)
0	0	1	1.7K Bytes (0100h – 07FFH)
0	1	0	2.7K Bytes (0100h – 0BFFH)
0	1	1	3.7K Bytes (0100h – 0FFFH)
1	0	0	6.7K Bytes (0100h – 1BFFH)
1	0	1	7.7K Bytes (0100h – 1FFFH)
1	1	0	8.2K Bytes (0100h – 21FFH)
1	1	1	8.5K Bytes (0100h – 22FFH)

CONFIGURE OPTION 2 : ROM Address 001FH

.7	.6	.5	.4	.3	.2	.1	.0
R_P	HL	VAPEN	–	–	–	–	RSTS

Initial value: 00H

R_P Read Protection

0 Disable “Read protection”

1 Enable “Read protection”

HL Hard-Lock

0 Disable “Hard-lock”

1 Enable “Hard-lock”

VAPEN Vector Area (00H – FFH) Protection Enable/Disable

0 Disable Protection (Erasable by instruction)

1 Enable Protection (Not erasable by instruction)

RSTS RESETB Select

0 P62 port

1 RESETB port with a pull-up resistor