
8-BIT MCU INTEGRATING 12-BIT ADC & LCD

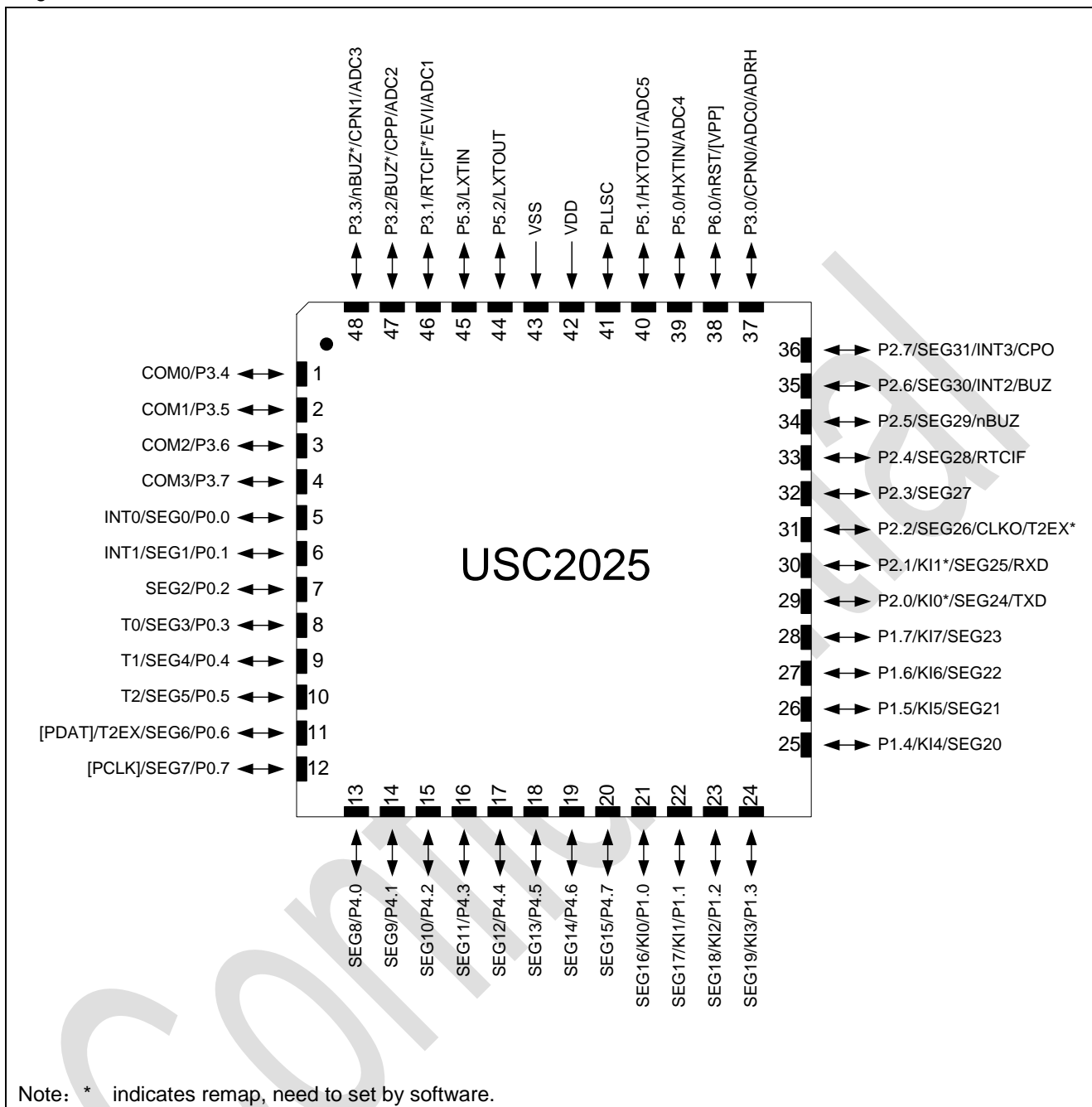
1. DESCRIPTION

USC2025 is a 8-bit MCU based on enhanced 51 core. It integrated 6+2-Ch/12bit-ADC and 128-seg LCD, embeds 16K-byte OTP and 512-byte RAM, also PLL, RTC, UART, Comparator and Timers/Counters.

Features

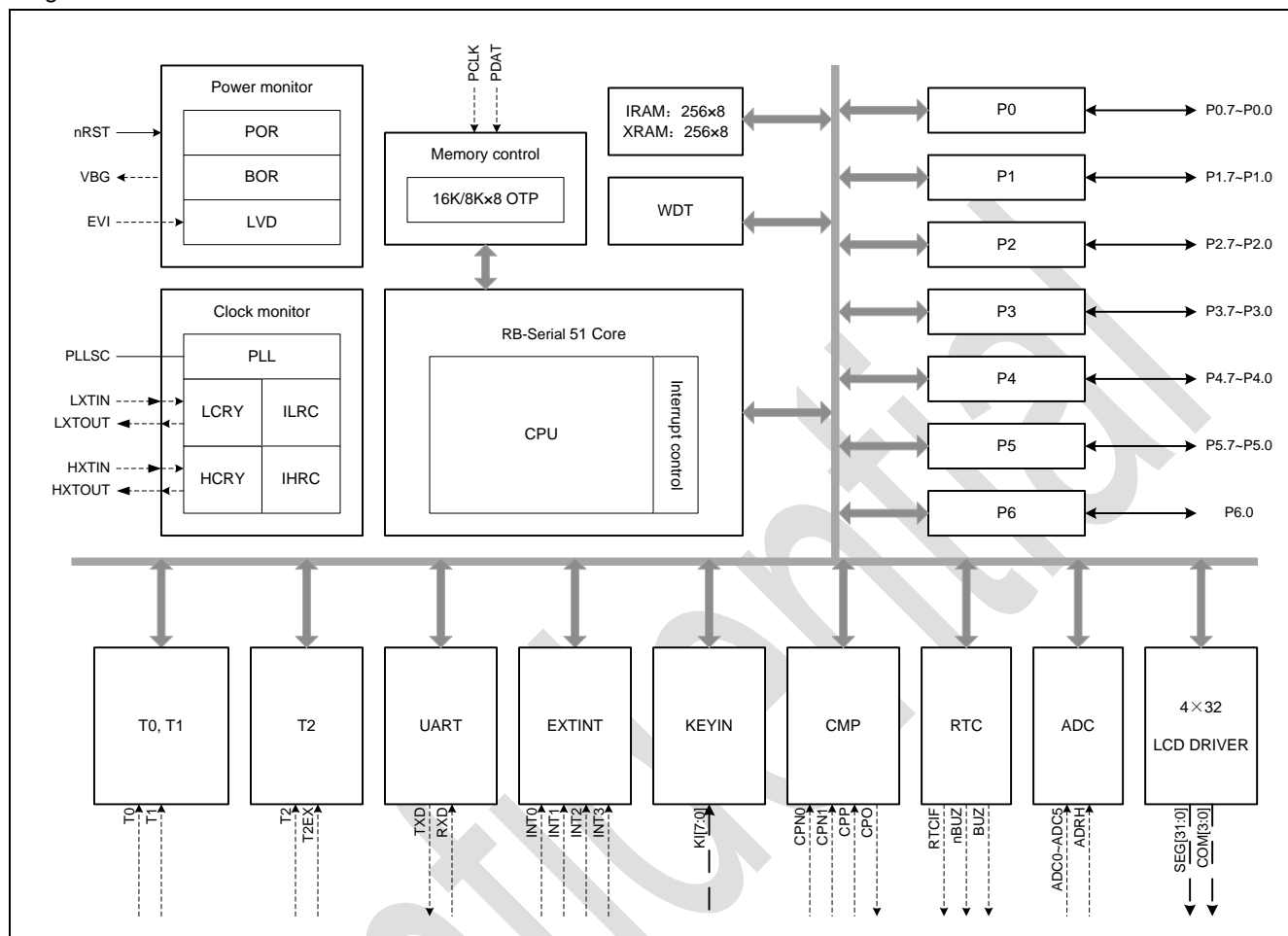
- Power supply and Reset
 - ✧ Built-In Power-On-Reset (POR).
 - ✧ Built-In Brown-Out-Reset (BOR) with 2 levels selectable.
 - ✧ Built-In Low-Voltage-Detect (LVD) with 8 levels selectable.
 - ✧ Built-in watchdog (WDT).
- CPU
 - ✧ 8-bit 51 Core, Compatible with C8051.
 - ✧ Software trap supported.
 - ✧ Dual DPTR.
- Clock monitor
 - ✧ Built-In 8MHz High precision Oscillator (IHRC), $\pm 5\%$ @ $-40\sim 85^{\circ}\text{C}$, $\pm 2\%$ @ $-10\sim 50^{\circ}\text{C}$.
 - ✧ Built-In 30KHz low frequency Oscillator (ILRC).
 - ✧ External High frequency Oscillator HCRY, $1\sim 8\text{MHz}@ \geq 2.4\text{V}$.
 - ✧ External Low frequency Oscillator LCRY, 32768Hz.
 - ✧ Built-In PLL, based on LCRY.
 - ✧ CPU maximum operating frequency: 4MHz @ 1.8~3.6V; 8MHz @ 2.4~3.6V.
 - ✧ System clock pre-divider: 1/2/4/8.
- Memory control
 - ✧ 16K-byte OTP, data retention time > 10 years.
 - ✧ OTP page encryption supported.
 - ✧ 512-byte RAM.
 - ✧ In-System-Programming (ISP) supported, only 5-pins are needed (including VDD/VSS).
- I/O
 - ✧ 45 I/O ports, P6.0 only open-drain when output.
- Peripherals
 - ✧ 8-channel keyboard input, can wake up MCU from PD mode.
 - ✧ 4-channel external interrupt input, can wake up MCU from PD mode.
 - ✧ 12-bit 6+2 channel ADC, maximum conversion rate: 100Ksps. Reference can be input from external pin.
 - ✧ 1-channel Comparator.
 - ✧ Three 16-bit standard Timer/Counter (T0,T1,T2).
 - ✧ 1-channel UART.
 - ✧ Limited version Real-Time-Clock, RTC.
 - ✧ 128-seg (4COM×32SEG) LCD.
- Low power modes
 - ✧ IDL mode.
 - ✧ PD mode.
- Package Type
 - ✧ 48-pin LQFP.
- Application
 - ✧ Panel display.
 - ✧ Medical and health care equipments.
 - ✧ smart metering.

Fig 3-2: USC2025 PIN CONFIGURATION



4. BLOCK DIAGRAM

Fig 4-1: BLOCK DIAGRAM



5. PIN MULTIPLEXING

Table 5-1: PIN MULTIPLEXING

I/O		LQFP48 -LL			BASIC	TIMER	UART	EXTINT	KEYIN	CMP	ADC	RTC	LCD
P3.4		1			-	-	-	-	-	-	-	-	COM0
P3.5		2			-	-	-	-	-	-	-	-	COM1
P3.6		3			-	-	-	-	-	-	-	-	COM2
P3.7		4			-	-	-	-	-	-	-	-	COM3
P0.0		5			-	-	-	INT0	-	-	-	-	SEG0
P0.1		6			-	-	-	INT1	-	-	-	-	SEG1
P0.2		7			-	-	-	-	-	-	-	-	SEG2
P0.3		8			-	T0	-	-	-	-	-	-	SEG3
P0.4		9			-	T1	-	-	-	-	-	-	SEG4
P0.5		10			-	T2	-	-	-	-	-	-	SEG5
P0.6		11			-	T2EX	-	-	-	-	-	-	SEG6
P0.7		12			-	-	-	-	-	-	-	-	SEG7
P4.0		13			-	-	-	-	-	-	-	-	SEG8
P4.1		14			-	-	-	-	-	-	-	-	SEG9
P4.2		15			-	-	-	-	-	-	-	-	SEG10
P4.3		16			-	-	-	-	-	-	-	-	SEG11
P4.4		17			-	-	-	-	-	-	-	-	SEG12
P4.5		18			-	-	-	-	-	-	-	-	SEG13
P4.6		19			-	-	-	-	-	-	-	-	SEG14
P4.7		20			-	-	-	-	-	-	-	-	SEG15
P1.0		21			-	-	-	-	KI0	-	-	-	SEG16
P1.1		22			-	-	-	-	KI1	-	-	-	SEG17
P1.2		23			-	-	-	-	KI2	-	-	-	SEG18
P1.3		24			-	-	-	-	KI3	-	-	-	SEG19
P1.4		25			-	-	-	-	KI4	-	-	-	SEG20
P1.5		26			-	-	-	-	KI5	-	-	-	SEG21
P1.6		27			-	-	-	-	KI6	-	-	-	SEG22
P1.7		28			-	-	-	-	KI7	-	-	-	SEG23
P2.0		29			-	-	TXD	-	-	-	-	-	SEG24
P2.1		30			-	-	RXD	-	-	-	-	-	SEG25
P2.2		31			CLKO	T2EX*	-	-	-	-	-	-	SEG26
P2.3		32			-	-	-	-	-	-	-	-	SEG27
P2.4		33			-	-	-	-	-	-	-	RTCIF	SEG28

I/O	LQFP48 -LL	BASIC	TIMER	UART	EXTINT	KEYIN	CMP	ADC	RTC	LCD
P2.5	34	-	-	-	-	-	-	-	nBUZ	SEG29
P2.6	35	-	-	-	INT2	-	-	-	BUZ	SEG30
P2.7	36	-	-	-	INT3	-	CPO	-	-	SEG31
P3.0	37	VBG	-	-	-	-	CPN0	ADC0/ADRH	-	-
P6.0	38	nRST	-	-	-	-	-	-	-	-
P5.0	39	HXTIN	-	-	-	-	-	ADC4	-	-
P5.1	40	HXTOUT	-	-	-	-	-	ADC5	-	-
PLLSC	41	PLLSC	-	-	-	-	-	-	-	-
VDD	42	VDD	-	-	-	-	-	-	-	-
VSS	43	VSS	-	-	-	-	-	-	-	-
P5.2	44	LXTOUT	-	-	-	-	-	-	-	-
P5.3	45	LXTIN	-	-	-	-	-	-	-	-
P3.1	46	EVI	-	-	-	-	-	ADC1	RTCIF*	-
P3.2	47	-	-	-	-	-	CPP	ADC2	BUZ*	-
P3.3	48	-	-	-	-	-	CPN1	ADC3	nBUZ*	-

Note1: * indicates remap, need to set by software.

6. PIN DESCRIPTION

Table 6-1: PIN DESCRIPTION

Module	PIN name	PIN type	Function description
Power supply	V _{DD}	P	Power supply
	V _{SS}	P	Ground
In-System-Programming (ISP)	PCLK	I	Programming clock Input
	PDAT	I/O	Programming data input/output
BASIC	LXTIN	I	External low frequency oscillator input
	LXTOUT	O	External low frequency oscillator output
	HXTIN	I	External high frequency oscillator input
	HXTOUT	O	External high frequency oscillator output
	PLLSC	A	PLL stabilization control pin
	CLKO	O	Clock output
	nRST	I	External reset input, low active
	VBG	A	Voltage of Band-gap output
EVI	A	External voltage input for LVD	
I/O	P0.0~P0.7	I/O	I/O ports, bit operation available
	P1.0~P1.7	I/O	I/O ports, bit operation available
	P2.0~P2.7	I/O	I/O ports, bit operation available
	P3.0~P3.3	I/O	I/O ports, bit operation available

Module	PIN name	PIN type	Function description
	P3.4~P3.7	I/O	I/O ports, bit operation available
	P4.0~P4.7	I/O	I/O ports, bit operation not available
	P5.0~P5.4	I/O	I/O ports, bit operation not available
	P6.0	I/O	I/O ports, bit operation not available. Open-drain only when output.
T0/T1/T2	T0/T1	I	Timer/counter 0/1 external counting clock input
	T2	I	Timer/counter 2 external counting clock input
	T2EX	I	Timer/counter 2 external control input
UART	TXD	O	UART data transfer port
	RXD	I	UART data receive port
EXTINT	INT0~INT3	I	External interrupt 0~3 input
KEYIN	KI0~KI7	I	Keyboard input, can wakeup MCU
CMP	CPP	A	Analog comparator 0 positive input
	CPN0	A	Analog comparator 0 negative input 0
	CPN1	A	Analog comparator 0 negative input 1
	CPO	O	Analog comparator 0 output
ADC	ADC0~ADC5	A	ADC input 0~5
	ADRH	A	ADC reference input
RTC	RTCIF	O	RTC interrupt flag output
	BUZ	O	Buzzer output, complementation output
	nBUZ	O	
LCD	COM0~COM3	O	LCD drive common pin
	SEG0~SEG31	O	LCD drive segment pin

7. ABSOLUTE MAXIMUM RATINGS

Table 7-1: ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Range	Unit
Supply voltage	V_{DD}	-0.3 ~ +5.0	V
Input voltage	V_I	-0.3 ~ $V_{DD}+0.3$	V
Total Sink Current	$\sum I_{OL}$	400	mA
Total Source Current	$\sum I_{OH}$	-320	mA
Storage temperature	T_{STG}	-40 ~ +125	°C
Operating temperature	T_{OPR}	-20 ~ +70	°C

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8. DC ELECTRICAL CHARACTERISTICS (unless otherwise specified, $V_{DD}=3V$, $T_a=25^\circ C$)

8.1. Power supply characteristics

Table 8-1: Power supply characteristics

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit		
Typical condition: $V_{DD}=5.0V$, $T_a=25^\circ C$. Temperature=-40~85°C, all IO output low, no load.								
Operating voltage	V_{DD}	$M_{CLK} \leq 8MHz$	2.4	-	3.6	V		
		$M_{CLK} \leq 4MHz$	1.8	-	3.6			
Operating Current, considering the temperature	I_{DD}	$F_{sysclk}=IHRC$	$M_{CLK}=4MHz$	$V_{DD}=3.0$	-	1.3	-	mA
				$V_{DD}=1.8$	-	0.8	-	
			$M_{CLK}=8MHz$	$V_{DD}=3.0$	-	2.5	-	
				$V_{DD}=2.4$	-	2.0	-	
		$F_{sysclk}=HCRY$	$M_{CLK}=4MHz$	$V_{DD}=3.0$	-	2.1	-	
				$V_{DD}=1.8$	-	1.0	-	
			$M_{CLK}=8MHz$	$V_{DD}=3.0$	-	3.2	-	
				$V_{DD}=2.4$	-	2.3	-	
		$F_{sysclk}=PLL$	$M_{CLK}=4.194MHz$	$V_{DD}=3.0$	-	1.5	-	
				$V_{DD}=1.8$	-	0.9	-	
			$M_{CLK}=2.097MHz$	$V_{DD}=3.0$	-	0.9	-	
				$V_{DD}=1.8$	-	0.5	-	
			$M_{CLK}=1.049MHz$	$V_{DD}=3.0$	-	0.6	-	
				$V_{DD}=1.8$	-	0.4	-	
		$M_{CLK}=0.524MHz$	$V_{DD}=3.0$	-	0.4	-		
			$V_{DD}=1.8$	-	0.3	-		
		$F_{sysclk}=LCRY$	$M_{CLK}=32768Hz$	$V_{DD}=3.0$	-	55	-	uA
				$V_{DD}=1.8$	-	17	-	
$F_{sysclk}=ILRC$	$M_{CLK}=F_{ILRC}$	$V_{DD}=3.0$	-	50	-			
		$V_{DD}=1.8$	--	11	-			
IDL current	I_{IDL}	$F_{sysclk}=IHRC$	$M_{CLK}=4MHz$	$V_{DD}=3.0$	-	260	-	uA
				$V_{DD}=1.8$	-	160	-	
		$F_{sysclk}=HCRY$	$M_{CLK}=8MHz$	$V_{DD}=3.0$	-	950	-	
				$V_{DD}=2.4$	-	600	-	
		$F_{sysclk}=PLL$	$M_{CLK}=4.194MHz$	$V_{DD}=3.0$	-	350	-	uA
				$V_{DD}=1.8$	-	220	-	
		$F_{sysclk}=LCRY$	$M_{CLK}=32768Hz$	$V_{DD}=3.0$	-	5	-	
				$V_{DD}=1.8$	-	4	-	
$F_{sysclk}=ILRC$	$M_{CLK}=F_{ILRC}$	$V_{DD}=3.0$	-	2	-			
		$V_{DD}=1.8$	-	0.5	-			
PD current	I_{PD}	32768Hz LCRY+RTC+LCD enabled, others all disabled.	$V_{DD}=3.0$	-	5	-	uA	
			$V_{DD}=1.8$	-	4	-		
		All disabled.	$V_{DD}=3.0$	-	0.5	1.5		

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
		V _{DD} =1.8	-	0.5	-	

Note: All current were measured when the gain of HCRY/LCRY was set minimum.

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8.2. IO characteristics

Table 8-2: IO characteristics

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit	
Typical condition: $V_{DD}=5.0V$, $T_a=25^{\circ}C$.							
High input voltage	V_{IH}	P0/P1/P2/P3/P4/P5	$0.7V_{DD}$	-	V_{DD}	V	
		P6.0	$0.8V_{DD}$	-	V_{DD}		
Low input voltage	V_{IL}	P0/P1/P2/P3/P4/P5	0	-	$0.3V_{DD}$	V	
		P6.0	0	-	$0.2V_{DD}$		
Output source current	I_{OH}	$V_{OH}=0.9V_{DD}$	P0/P1/P2/P3.1~P3.7/P4/P5	-	4	-	mA
			P3.0	-	10	-	
Output sink current	I_{OL}	$V_{OL}=0.1V_{DD}$	P0/P1/P2/P3.1~P3.7/P4/P5	-	7	-	mA
			P3.0	-	11	-	
			P6.0	-	3	-	
Internal Pull-up resistor	R_{pu}	$V_{IN}=0V$	$V_{DD}=3.6V$	90	120	150	k Ω
			$V_{DD}=3.0V$	130	190	250	
			$V_{DD}=2.2V$	300	450	600	
Leakage current	I_{IL}	High-impedance input V_{DD}/V_{SS}	P0/P1/P2/P3/P4	-	-	± 10	nA
			P5	-	-	± 10	
			P6.0	-	-	± 10	
Effective pulse width (filtering)	$T_{PW}(IO)$	nRST	$V_{DD}=3.0V$	3	-	-	us
			$V_{DD}=1.8V$	3	-	-	us
		INT0~4 /K10~K17	$V_{DD}=3.0V$	3	-	-	us
			$V_{DD}=1.8V$	3	-	-	us

8.3. System monitoring and reset characteristics

Table 8-3: System monitoring and reset characteristics

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
Typical condition: $V_{DD}=5.0V$, $T_a=25^{\circ}C$.						
POR release voltage	V_{POR}^*	-	-	0.7	-	V
Bandgap voltage	V_{BG}		1.18	1.20	1.22	V
MVR output voltage	$T_{PW(nRST)}$		3	-	-	us
BOR voltage	V_{BOR}	BORS=0	-	1.7	-	V
		BORS=1	-	2.6	-	
BOR release hysteresis voltage	$V_{HYS(BOR)}$		-	50	-	mV
BOR operating current	I_{BOR}	IDL mode	-	32	-	uA
LVD voltage	V_{LVD}	VDS = 000	-	2.0	-	V
		VDS = 001	-	2.1	-	
		VDS= 010	-	2.2	-	
		VDS= 011	-	2.3	-	
		VDS= 100	-	2.4	-	
		VDS = 101	-	2.7	-	
		VDS= 110	-	3.0	-	
		VDS = 111	-	3.2	-	
LVD release hysteresis voltage	$V_{HYS(LVD)}$	$V_{DD} \geq 2.4$	-	120	-	mV
		$V_{DD} < 2.4$	-	60	-	
LVD operating current	I_{LVD}	IDL mode	-	37	-	uA
POR reset delay time	T_{PWUT}		-	20	-	ms
BOR reset delay time	T_{DBOR}		-	0.4	-	
PD wake exit time	T_{PD}		-	110	-	us

Note : * indicates simulation value, not test.

8.4. Oscillation and clock characteristics

Table 8-4: Oscillation and clock characteristics

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
Typical condition: $V_{DD}=5.0V$, $T_a=25^{\circ}C$.						
Frequency of IHRC after calibration	F_{IHRC}	3.0V, $-20\sim 65^{\circ}C$	7.92	8	8.08	MHz
		3.0V, $-40\sim 85^{\circ}C$	7.84	8	8.16	
		2~3.6V, $-40\sim 85^{\circ}C$	7.6	8	8.4	
		1.8~3.6V, $-40\sim 85^{\circ}C$	6	8	8.4	
IHRC Start-up time	$T_{IHRCSTR}^*$	-	-	10	-	us
IHRC operating current	I_{IHRC}	Enable IHRC when MCik from ILRC @IDL, measure the current increasing value	-	80	-	uA
Frequency of ILRC	F_{ILRC}	1.8~3.6V, $-40\sim 85^{\circ}C$	10	30	50	KHz
		3.0V, $-40\sim 85^{\circ}C$	20	30	40	
ILRC Start-up time	$T_{ILRCSTR}^*$	-	-	60	-	us
ILRC operating current	I_{ILRC}	Enable ILRC @PD, measure the current increasing value	-	0.5	-	uA
Test condition for LCRY start-up time: $V_{DD}=1.8\sim 3.6V$; $-40\sim 85^{\circ}C$						
LCRY Start-up time	$T_{LCRYSTR}$	32768Hz, 12pF load connected to GND	-	500	2000	ms
LCRY operating current	I_{LCRY}	Enable LCRY @PD, measure the current increasing value	-	3	-	uA
Test condition for HCRY start-up time: $V_{DD}=1.8\sim 3.6V$; $-40\sim 85^{\circ}C$						
HCRY Start-up time	$T_{HCRYSTR}$	8MHz, 20pF load connected to GND	-	5	50	ms
HCRY frequency range	F_{HCRY}	$1.8 < V_{DD} < 2.0V$	1	-	8	MHz
		$V_{DD} > 2.4V$	1	-	16	
HCRY operating current	I_{HCRY}	Enable HCRY(4M) when MCik from ILRC @IDL, measure the current increasing value	-	330	-	uA
PLL reference clock frequency range	F_{PLLREF}	1.8~3.6V	30	32.768	40	KHz
PLL output frequency range	F_{PLL}	128 frequency doubling	-	4.194	-	MHz
PLL lock time	$T_{PLLLOCK}$	1.8~3.6V, $-40\sim 85^{\circ}C$	-	0.5	6	ms
PLL operating current, 4.194MHz	I_{PLL}	Enable PLL when MCik from ICRY @IDL, measure the current increasing value	-	700	-	uA

Note : * indicates simulation value, not test.

8.5. Comparator characteristics

Table 8-5: Comparator characteristics

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
Typical condition: $V_{DD}=5.0V$, $T_a=25^{\circ}C$, $V_{cm}=V_{DD}/2$.						
Input offset voltage (CPP rising edge)	V_{os}^*		-20	0	20	mV
Input common mode voltage	V_{cm}	Response time <200ns	0.7	-	$V_{DD}-0.7$	V
		Response time <500ns	0	-	V_{DD}	V
Common Mode Rejection Ratio	$CMRR^*$	Ambient temperature $25^{\circ}C$	-	1.5	-	mV/V
Comparator hysteresis voltage (CPP falling edge with hysteresis)	V_{hyster}		-	12	-	mV
Start-up delay time	T_{str}		-	0.6	2.0	us
Response time	rising edge	$V_{cm}=V_{DD}/2$ Overdrive voltage $\pm 0.1V$	-	30	300	ns
	falling edge		-	30	300	ns
Operating current	I_{cmp}	-	-	40	-	uA
CMPVR Stabilization time	T_{scvr}	-	-	1	-	us

Note : * indicates simulation value, not test.

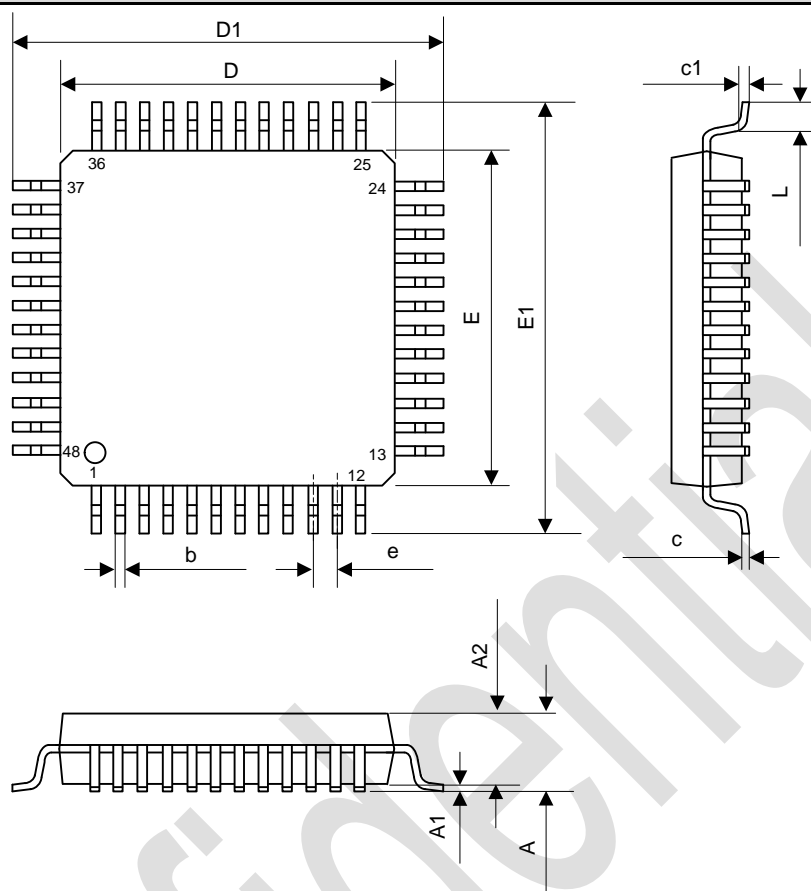
8.6. A/D converter characteristics

Table 8-6: ADC characteristics

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
Typical condition: $V_{DD}=5.0V$, $T_a=25^{\circ}C$.						
Resolution	NR		12			Bit
ADC operating voltage range	V_{DDAD}	$1MHz < F_{adclk} < 2MHz$	2.5	-	3.6	V
		$F_{adclk} < 1MHz$	2.0	-	3.6	V
Input analog voltage range	V_{ADIN}		0	-	V_{DDAD}	V
Sample & hold capacitor	C_{ADIN}		-	25	-	pF
Analog channel impedance	R_{ADIN}	$2.5V < V_{DDAD} < 3.6V$	-	1	10	k Ω
		$2.0V < V_{DDAD} < 2.5V$	-	-	100	k Ω
ADC clock frequency	F_{adclk}		-	-	2	MHz
ADC clock period	T_{AD}		0.5	-	-	μs
Sample time	T_{smp}	Enable by software	-	6.5	-	T_{AD}
Conversion time	T_{conv}		-	20	-	T_{AD}
ADC operating current	I_{DDAD}	$F_{adclk} = 2MHz$	-	200	-	μA
Differential nonlinearity	DNL	$2.5V < V_{DDAD} < 3.6V$ $F_{adclk} < 2MHz$	-	-	± 4	LSB
		$2.0V < V_{DDAD} < 3.6V$ $F_{adclk} < 1MHz$	-	-	± 4	LSB
Integral nonlinearity	INL		-	-	± 4	LSB
Offset error	E_{zs}		-	-	± 8	LSB
Gain error	E_{fs}		-	-	± 8	LSB
Global uncorrected error	E_{TUE}		-	-	± 8	LSB
No missing code digit	NMC		10			Bit

LQFP48-7x7-0.5

Unit:mm



Symbol	Min	Typ	Max
A			1.60
A1	0.05		0.20
A2	1.35		1.45
b	0.17		0.27
c	0.09		0.20
c1		0.25	
D	6.90		7.10
D1	8.80		9.20
E	6.90		7.10
E1	8.80		9.20
e		0.50 (BSC)	
L	0.40		0.75